Optical Interconnects at the Chip and Board Level – Challenges and Solutions

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Acknowledgements:
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Dr. Mani Sundaram, TeraConnect
System interconnect hierarchy

Inter-chip

Inter-board

Inter-shelf

Inter-rack

Network Element

Inter-site

Network Elements

Long-haul

Central office
Outline

➢ Bandwidth limitations of electrical interconnects
➢ Optical interconnect insertion points
➢ 10 Gbps products
➢ Free-space optical interconnects
➢ Convergence/divergence
➢ Conclusions
Problem statement

- Electrical interconnects do not have sufficient bandwidth to meet the interconnection requirements of future telecommunications and computing systems.
- Short distance interconnects will benefit from an optical solution.
- Multiple groups pursuing solutions:
  - Telecommunications equipment manufacturers
  - Computing systems manufacturers
  - Storage/disk farms
Limitations of electrical interconnects

- As data rates increase, electrical interconnects are limited by:
  - Power
  - Distortion
  - Cross-talk
  - Pin-out capacity

- Fundamental: aspect ratio limit:

\[
B_{\text{max}} \leq 10^{16} \times \frac{A}{l^2} \quad \text{(bit/s)}
\]
Opportunities for optical interconnects

- LAN/WAN
- Racks/chassis
- Longhaul

- VSR optical interconnects

**Distance Ranges:**
- 1mm
- 1cm
- 10cm
- 1m
- 10m
- 100m
- 1km
- 10km
- 100km
- 1000km

**Interconnect Technologies:**

- **CWDM and TDM:**
  - $\lambda$, time muxing
  - (single mode fiber, multimode fiber)

- **DWDM:**
  - $\lambda$, time muxing
  - (single mode fiber)
VSR application: intra-office
(D. Goodwill, Nortel Networks)

- 2 to 300 meter interconnect
- 10 Gbps
VSR optical interconnect technology requirements

- Interconnect opaque elements
- Large aggregate data rates (10, 40, 100 Gpbs)
- Multiple distance possibilities (2m to 10 km)
- Low power (< 3 W/10 Gbps)
- Standardized interfaces (electrical and optical)
- Low cost (~$100/Gbps)
Enabling VSR technologies

- Vertical Cavity Surface Emitting Lasers (VCSELs)
- Fiber (single/multi-mode)
- Connectorized optical interfaces
- Standardized electrical interfaces
VCSELs

- Optical cavity oriented normal to wafer.
- Current injection is efficient, slope efficiencies are high, and threshold currents are very low (sub 100 µA reported in late 1990s).
- AlGaAs-GaAs (850 nm) VCSELs are available at low cost.
- Current research on 1.3µm and 1.55µm devices.
VCSEL merits

- Inexpensive (Honeywell 850nm VCSEL $10)
- Bandwidths of 10Gbps at threshold currents of mA’s
- Wafer testable prior to doing any packaging
- Post-processing of mirrors not required
- Two-dimensional arrays available

1-D array

2-D array
Fiber types

**Single mode fiber**

- Distance \( r \)
- Core diameter
- Refractive index \( n \)

- Step index core
- Core diameter 8-10 µm
- Bandwidth-length product limited by chromatic dispersion
- Reach at 10 Gbps > 10’s of km

**Multimode fiber (GRIN)**

- Distance \( r \)
- Core diameter
- Refractive index \( n \)

- Gradient refractive index (GRIN) core
- Core diameter 50/62.5 µm
- Bandwidth-length product limited by intermodal dispersion
- Reach at 10 Gbps ≈ 60 m at 850 nm
VSR driver: 10 Gig Ethernet standards
(http://grouper.ieee.org/groups/802/3/ae/index.html)

• **3 Serial:**
  – 850 nm, 2m – 300m on high performance multi-mode fiber
  – 1310 nm, 2m – 10km on standard single mode fiber
  – 1550 nm, 2m – 40km on standard single mode fiber

• **1 Parallel:**
  – 4 wavelengths in the 1310 nm window (1269nm – 1355nm);
    2m – 300m on MMF; 2m – 10km on SMF

• Current products use 850nm VCSELs and 1310nm DFBs; 1310nm VCSELs coming on fast.
VCSEL based 10 Gbps optical module
(D. Kabal and M. Ayliffe, Picolight)

• **Applications:**
  – 10 Gigabit Ethernet (WAN and LAN)
  – OIF VSR OC-192
  – Router interconnection
  – Computer cluster cross connects

• **Low power:** < 6 W
• **0** to 70 C
• **2** – 300 meters
• **50/125 μm** MMF
10.7 Gpbs 850 nm VCSEL
(D. Kabal and M. Ayliffe, Picolight)
Current products: channels vs. data rate

- **Data rate (Gb/s)**
  - 40 Gbps to follow
  - 10 Gbps

- **Number of channels**
System interconnects

- Inter-rack
- Inter-site
- Inter-shelf
- Inter-board
- Inter-chip

“Inside the box”

Network Elements

Central office
Opportunities for optical interconnects

2-D VSR optical interconnects

- Longhaul
- LAN/WAN
- Racks/chassis
- Inter-shelf
- Inter-Board
- Inter-Chip

2D SDM & TDM: space, time muxing
(CWDM, parallel fiber)

CWDM & TDM: λ, time muxing
(single mode fiber, multimode fiber)

DWDM: λ, time muxing
(single mode fiber)
2-D Free Space Optical Interconnects

- Free Space Optical Interconnect (FSOI) bandwidths achieved through Time Division Multiplexing (TDM) and Space Division Multiplexing (SDM).
- Connection densities >2000 connections/cm² at > 1Gbps per connection.
- OE-VLSI ASIC baseline functions: Electrical-to-Optical (E-O); Optical-to-Electrical (O-E); Optical-to-Electrical-to-Optical (O-E-O) data conversion.
Application: free-space optical backplane
Application: chip-to-chip/board-to-board

International Technology Roadmap for Semiconductors

<table>
<thead>
<tr>
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<td>Technology node</td>
<td>180 nm</td>
<td>120 nm</td>
<td>100 nm</td>
<td>70 nm</td>
<td>50 nm</td>
<td>35 nm</td>
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<td>Density (M/cm²)</td>
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<td>350</td>
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<td>Chip size (mm²)</td>
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<td>On-chip clock (MHz)</td>
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<td>Off-chip high-speed pins</td>
<td>700</td>
<td>1,500</td>
<td>1,900</td>
<td>2,300</td>
<td>2,700</td>
<td>3,000</td>
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<tr>
<td>Off-chip speed (MHz)</td>
<td>600</td>
<td>862</td>
<td>1,000</td>
<td>1,250</td>
<td>1,500</td>
<td>1,800</td>
</tr>
</tbody>
</table>

(Data for high-performance market segment)
Application: chip-to-chip/board-to-board


International Technology Roadmap for Semiconductors

<table>
<thead>
<tr>
<th>Year of Introduction</th>
<th>Density (M/cm²)</th>
<th>Chip size (mm²)</th>
<th>On-chip clock (MHz)</th>
<th>Off-chip high-speed pins</th>
<th>Off-chip speed (MHz)</th>
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<tr>
<td>2008</td>
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<td>2,300</td>
<td>1,250</td>
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<td>2,700</td>
<td>1,500</td>
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<tr>
<td>2014</td>
<td>35 nm</td>
<td>2,130</td>
<td>13,500</td>
<td>3,000</td>
<td>1,800</td>
</tr>
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</table>

‘No known solution’
Chip-to-chip requirements

Data rate (Gb/s)

Number of channels

5 Tbps (2014)

On-chip clock (13.5 Gbps)

Off-chip bus (1.8 Gbps)

40 Gbps

10 Gbps

1000

100

10

1

10000

1000

100

10

1
2-D VSR optics: open issues

- Total interconnect capacity
- Number of channels/data rate per channel
- Length
- Optoelectronics
- Optics
Starting Assumptions

• 2D VCSELs and photodiodes arrays @ 850 nm, mW’s.
• OED Pitch: 125 µm
• CMOS, SiGe, UTSi electronics
• Interconnect distances: 5 – 100 mm
• FSOI optical interconnect insertion loss < 3 dB
Optoelectronic-VLSI

Multichip TXER module

Heterogeneous integration

CMOS chip
Driver
VCSEL Array

OE-VLSI

Increased parallelism
Reduced power dissipation
ASIC #1) 256 VCSEL/PD OE-VLSI ASIC
(D.V. Plant et al, JLT, 19, 2001)

10mm x 10 mm, 0.35 µm TSMC CMOS
Designed as Network Interface Chip

- Pitch within cluster: 125 µm
- Cluster pitch: 750 µm
- 2844 channels/cm
- \textit{Performed 3 functions: E-O, O-E, and O-E-O}

OEO operation at a) 250 Mbps; b) 400 Mbps.
ASIC #2) 1080 VCSEL/PD OE-VLSI ASIC
(M.B. Venditti et al, in press, JSTQE, 2003)

14.6 x 7.5 mm 0.25 μm TSMC CMOS (5 metal, single poly, n-well)
Signal Processing Functions

- Transceiver/transponder
- Clock acceleration
- Parallel Forward Error Correction (FEC)
- On chip data generation (testing)
Test and Verification

Toggle

Blink

Random

Close-up
## OE-VLSI ASIC Comparison

<table>
<thead>
<tr>
<th></th>
<th>ASIC #1</th>
<th>ASIC #2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optical I/O</td>
<td>256 (single ended)</td>
<td>540 (differential)</td>
</tr>
<tr>
<td>Electrical I/O</td>
<td>32 (single ended)</td>
<td>128 (single ended)</td>
</tr>
<tr>
<td>Transceivers</td>
<td>Single ended</td>
<td>Fully differential</td>
</tr>
<tr>
<td>Total power dissipation</td>
<td>~ 100 mW/ch</td>
<td>~ 35 mW/ch</td>
</tr>
<tr>
<td>(calculated)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Connection density</td>
<td>2844 chs/cm²</td>
<td>6800 chs/cm²</td>
</tr>
<tr>
<td>Number of functions</td>
<td>Transceiver &amp; transponder</td>
<td>Transceiver/transponder; clock acceleration, FEC, self-test</td>
</tr>
</tbody>
</table>
Optically Interconnected PCBs

- Backplane OE-VLSI ASICs perform:
  - E-O, O-E, and O-E-O data conversion
  - Backplane level signal processing functions such as a) address recognition, b) clock acceleration, c) FEC
Chip-to-Chip Interconnect

- Forms basis of technologies to be discussed:
  - VCSELs/PDs & heterogeneous integration
  - OE-VLSI ASICS (transceivers, layout, signal processing)
  - Packaging and optics
2-D VSR optical interconnects: design choices

• Critical design parameters:
  – Optical throw
  – Number of channels
  – Array area
  – Misalignment tolerance
  – Source characteristics

• These cannot all be optimized independently
Optical relay choices

**Microchannel**
- Short throw (diffraction limited)
- Simple lenses
- Tight lateral tolerances

**Clustered (minilens)**
- Longer throw
- More complex optical design
- Improved lateral tolerances

**Macrolens**
- Maximum throw
- Stresses field of view
- Aberration-limited
Optical relay choices

- Longer throw
- More complex optical design
- Improved lateral tolerances
Design for misalignment tolerance

- Misalignment results from manufacturing and assembly errors
- Systems designed to be tolerant to misalignment
- Calculate the impact of misalignment on performance
Design for misalignment tolerance

- Misalignment results from manufacturing errors, assembly
- Systems should be tolerant to misalignment
- Calculate the impact of misalignment on performance
- *What happens when all components are misaligned?*
  - A Monte-Carlo simulation is required
Modularization

• Typically systems have components that have critical alignment tolerances

• This requires that the system is assembled as a series of modules

• Each module is comprised of components that must be mutually aligned with care – tight tolerance

• Ideally the modules can then be assembled with passive mechanical alignment – loose tolerance
Example: 512 channel optical board to board link

- 86 mm throw
- 3x6 mm active area
- 256 channels (bidirectional)
- \( \rightarrow \) Clustered optical design

(M. Châteauneuf et al, Optics in Computing 2001, pp.64-66.)
512 channel parallel optical board to board link

- 86 mm throw
- 3x6 mm active area
- 256 channels (bidirectional)
- → Clustered optical design

(M. Châteauneuf et al, Optics in Computing 2001, pp.64-66.)
Assembly and packaging

• Module assembly techniques include:
  – Interferometric techniques
  – In situ alignment techniques
  – Active alignment

• Module integration requires molded or machined features
Packaging challenge and solutions

- Machined frame
- Ceramic spacers
- Mechanical alignment features
- Alignment lenses
- Microlens array
- Relay lenses
- Relay block
Completed 256 channel bidirectional system*

Opportunities for optical interconnects

1D, 2D VSR optical interconnects

Inter-Chip
Inter-Board
Inter-shelf

1mm 1cm 10cm 1m 10m 100m 1km 10km 100km 1000km

1D, 2D VSR optical interconnects

2D SDM & TDM: space, time muxing
(CWDM & TDM: λ, time muxing

(FSOI, parallel fiber) (single mode fiber, multimode fiber)

DWDM: λ, time muxing
(single mode fiber)
### VSR optical interconnect requirements

<table>
<thead>
<tr>
<th>Number of channels</th>
<th>Data rate (Gb/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>100</td>
<td>1000</td>
</tr>
<tr>
<td>1000</td>
<td>10000</td>
</tr>
<tr>
<td>10000</td>
<td>1</td>
</tr>
</tbody>
</table>

#### Key Points:
- **Data rates**: 40 Gbps, 10 Gbps, 5 Tbps, 2-D FSOI (13.5 Gbps), Off-chip bus (1.8 Gbps)
- **Interconnects**: 1,2-D Fiber, 2-D FSOI, 2-D fiber, Xanoptix, Teraconnect, McGill/CITR
Convergent challenges

- VCSELs with low threshold currents ($I_{th}$)
- Low loss optical interconnect
- Low power consumption
- Non-amplified link
- Low cost
### Divergent challenges

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Telecom</th>
<th>Computing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate per channel</td>
<td>10 – 100 Gbps</td>
<td>1 – 10 Gbps</td>
</tr>
<tr>
<td>Length</td>
<td>Meters to kilometers</td>
<td>Millimeters to meters</td>
</tr>
<tr>
<td>Interconnect topology</td>
<td>Moderate &amp; 1D (100’s connections)</td>
<td>High and 2D (100’s to 1000’s of connections)</td>
</tr>
<tr>
<td>Optical medium</td>
<td>Fiber (SM/MM)</td>
<td>2-D; FSOIs, parallel fiber</td>
</tr>
<tr>
<td>Connectorization</td>
<td>Yes</td>
<td>Desirable</td>
</tr>
<tr>
<td>Electrical interface</td>
<td>Serial/de-serial</td>
<td>Directly from ASIC</td>
</tr>
</tbody>
</table>
Conclusion

- Optical interconnects continue to penetrate systems
- New solutions for shorter reaches required
References


