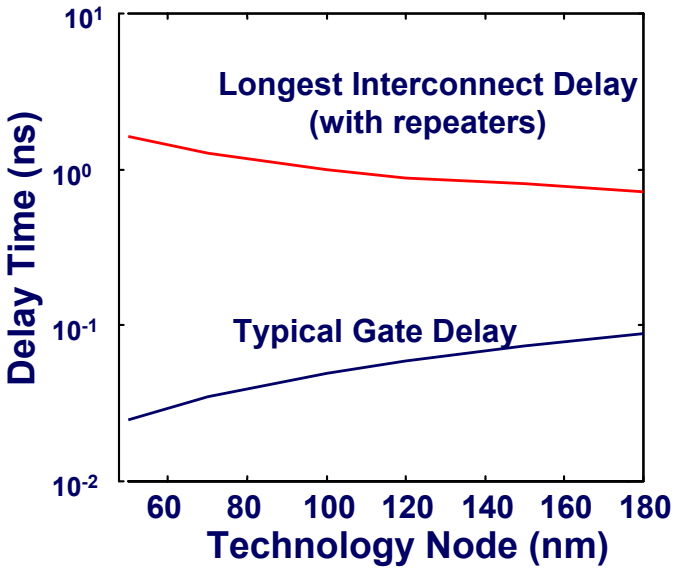
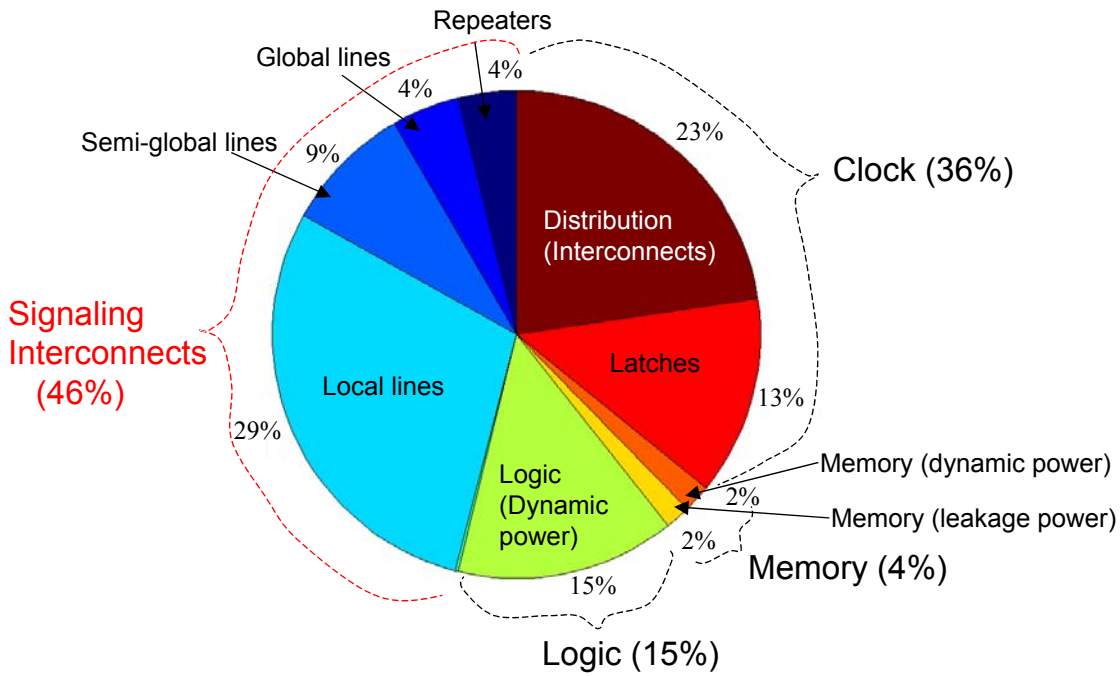
Conventional Interconnects: Challenges and Limitations

- Metal interconnect delay is increasing
- Interconnect power (CV^2f) also rises in future
- Bit rate α A/L^2 is becoming a limit

DELAY

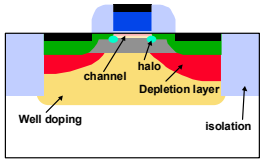


POWER



Technology Progression

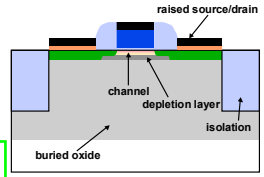
Bulk CMOS



Cu interconnect

Low-*k* ILD

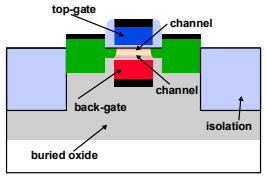
FD SOI CMOS



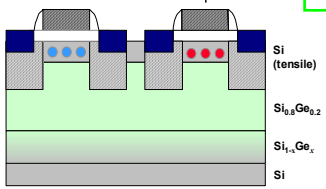
Metal gate

High *k* gate dielectric

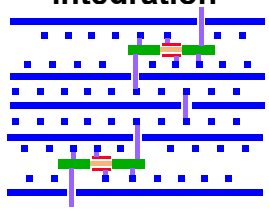
Double-Gate CMOS



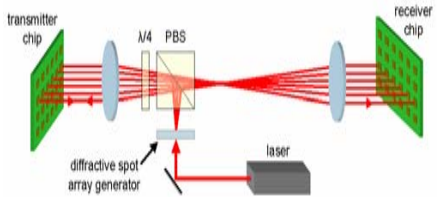
Strained Si
Ge channel



3D, heterogeneous integration



Optical interconnect



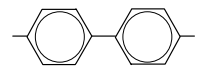
Detectors, lasers, QWM, waveguides

Nanotechnology

Self-assembly

Nanotube

Interconnects and contacts for nanodevices



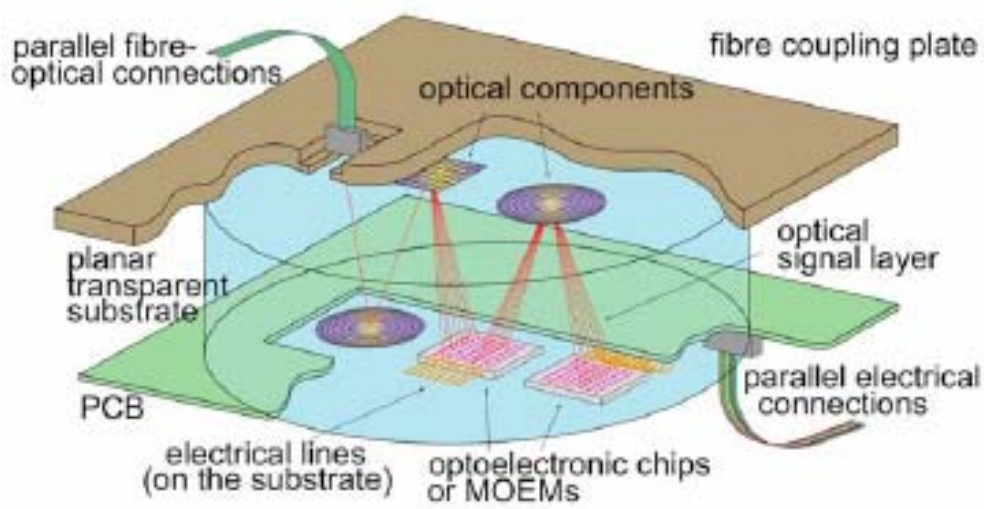
Molecular devices

100 nm → 2 nm

Feature Size

Can Optical Interconnects help?

- **Signal wires**
  - **Reduce delay**
  - **Increase bandwidth**
- **Clock distribution**
  - **Reduce delay variation**
    - **jitter and skew**
  - **Lower power?**
    - **Simplified clock distribution**
    - **Avoid on-chip repeaters**
    - **Off-chip drivers**



(Jurgen Jahns, Fernuniversitätt Hagen, Germany)

Economics and not the technology will dictate integration of optical interconnects on Si ICs