Conventional Interconnects: Challenges and Limitations

- Metal interconnect delay is increasing
- Interconnect power \((CV^2f)\) also rises in future
- Bit rate \(\alpha A/L^2\) is becoming a limit

### DELAY

![Delay Time Graph]

- Longest Interconnect Delay (with repeaters)
- Typical Gate Delay

### POWER

![Power Pie Chart]

- Clock (36%)
- Local lines
- Latches
- Logic (Dynamic power)
- Memory (dynamic power)
- Memory (leakage power)
- Repeaters
- Semi-global lines
- Global lines

Signaling Interconnects (46%)
Technology Progression

Bulk CMOS
- Well doping
- Depletion layer

FD SOI CMOS
- Raised source/drain
- Buried oxide

Double-Gate CMOS
- Top-gate
- Bottom-gate
- Buried oxide

Optical interconnect
- Detectors, lasers, QWM, waveguides
- Optical interconnect

Strained Si Ge channel
- Self-assembly
- Interconnects and contacts for nanodevices

Nanotechnology
- Nanotube
- Molecular devices

Feature Size
- 100 nm
- 2 nm

Technology Trends
- High k gate dielectric
- Metal gate
- Cu interconnect
- Low-k ILD

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Can Optical Interconnects help?

• Signal wires
  ‣ Reduce delay
  ‣ Increase bandwidth

• Clock distribution
  ‣ Reduce delay variation
    – jitter and skew
  ‣ Lower power?
    – Simplified clock distribution
    – Avoid on-chip repeaters
    – Off-chip drivers

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Economics and not the technology will dictate integration of optical interconnects on Si ICs