Silicon Based System in Package  
[Beyond System on Chip] 

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The Electronics Industry is CONSUMER DRIVEN

The consumer’s needs drive the OEM to provide “smaller, faster, cooler”

The OEM drives the industry to innovate.

“System in Package” is the required innovation for the next decade.
Moore’s Law is Alive and...well?…

The entire world disappears into a black hole in 2015......
Improving materials and processes to increase density only satisfy one direction.

Complexity adds demands on the rest of the food chain.
SoC Technology relies on novel IP and Integration Strategies

- Complex IC Design Tools
- Verification Methodologies
- IP “reuse”
- **Homogeneous Semiconductor Material**
• System = Hardware + Software + Application
• Hardware/Software partitioning is crucial
• The SoC Challenges
  – reuse and easy integration
  – faster time-to-market and smaller circuit geometry
  – high performance and low power
  – all of the above @ low cost

• The Solution - Innovative Architectures, Design Methodologies and Tools
  – they will drive the SoC revolution
  – handcrafting to squeeze the last picoseconds and the last thousands gates are a thing of the past

Source: Quarc, Hotchips 2000
In the 80’s, ASICs displaced TTL.

In the 90’s ASIC methodology fundamentally changed the way ICs were designed.

In the next few years, System in Package technology will fundamentally change the way ICs and systems are designed and manufactured.
Where Are We REALLY Going?

Source: TI

Computing - Controlling => Communicating - Storing

We are hunters…

We are gatherers…
Figure 1: Prior to 1997, Internet traffic had been doubling every year on average. It's now growing 4 times annually on average. Source: Caspian Networks analysis.
**Target Markets**

- **DP / Consumer**
  - Notebook PC
  - Portable digital

- **Communications**
  - LAN/WAN switching
  - Electro-Optic PHY

**System Level ASIC/ASSP Market**

Source, Gartner Group, 2000
- Very High Bandwidth (Tb/s)
- Reduced system cost
- Fast, economical design flow
- Increased functionality
- Reduced footprint, power, noise
- High testability

Multi-Level Integration is a Clear Path
SiP optimization of ICs creates breakthroughs in system cost and performance

- High speed, low power I/O
- High density I/O
- Simplified IC processing
- Reduced IC area
- Better Memory Granularity
High Capacity “DieCore™”
- 9Mb (128k x 36(x6) x 2) Q2/2001
- 18Mb (256k x 36(x6) x2) Q4/2001

Extremely High Bandwidth per die
- 250 Gb/s peak (10x competition)
- Six independent data ports
- This bandwidth for 1W!

Current Technologies
- 0.18um, .15um

Embedded SRAM bandwidth benefit in a separate die level solution
**DRAM bandwidth benefit of embedded solution in a silicon part**

- High capacity die
  - 64/128Mb (512k x 32 x 4)

- High bandwidth
  - 100Gb/s peak bandwidth (8x RAMBUS)
  - Quad port (16 bank) concurrent access
  - Low Latency core- 20 nS random row

- Current technology
  - 0.17um from memory partner
  - samples Q4/2001
ÖSiP Technology leverages existing Integration Strategies

- MCM / PCB Tools
- Methodologies
- Heterogeneous Semiconductor Materials

FloorPlan MicroBoard

Automatic Routing

MicroPallet Creation

Verification & GDSII
Ü Chip-sized routing substrate
  - High yield, small footprint

Ü Silicon BGA
  - High performance package
  - Low profile form factor

Ü Integrated passive components
  - Increase performance and value
  - example: 350-500 nF/cm² for core decoupling

*Patented solution for multi-chip integration*
**Applying IC technology to interconnect**

- **Microelectronic fabrication**
  - Low cost, high density routing
  - 25um trace and via pitch

- **High speed copper routing**
  - 50Ω transmission line
  - ~50pS / cm propagation delay
  - low k dielectric @ 2.65

- **Integrated solder bump**
  - 125um I/O pitch = >5000 I/O per cm²
  - 50 pH per bump inductance
  - bump is on less expensive wafer
Wafer level solution to optimize yield

- Wafer level handling
  - Eliminate bare die damage

- Wafer level flip-chip attach
  - High throughput process

- Wafer level test
  - Eliminate compound yield loss
Integrate multiple ICs to eliminate PCB interconnect & area

- From existing die, without redesign:
  - 30-50% performance increase
    (example: 225MHz -> 340MHz)
  - 30-50% power decrease
    (Example: 24W -> 18W)
  - 400% PCB area decrease
    (Example: 10 sq inch -> 2.5 sq inch)
  - EMI attenuation
    System power noise coupling into signal lines reduced
Solution: Eliminate components from motherboard

- Lower system cost
  - 5 fewer packages
  - 2 fewer routing layers
  - 900 fewer solder joints
  - 35 fewer passives
  - No DIMM socket

- Lower power by
  - 475 mWatt
“Pure” SoC vs SiP:

• Save typically 3-4 metal layers in stand alone SRAM memory vs “route over” layers required in embedded memory........ Whether they are used or not!

• Save all the trench cell, special implant layers, special metal patterning rules associated with embedded DRAM. 10 mask steps of cost burden on logic gates removed

• Memory portion of design is not burdened with defects in logic portion which aren’t repairable
• Burn In only the die/pallet combinations that need it. No compounding burden for the SiP from burnin

• Tester costs vastly reduced: only test memory on less expensive memory tester. Logic portion of system not “sitting in test” while analog & special functions tested.

• “WHAT A CONCEPT”: design in appropriate technology!
  > use SiGe for the high speed logic,
  > use DRAM process for DRAM,
  > use .35u trailing CMOS for analog @ 5V
  >(InP, GaAs, .......)
It is uniformly **less expensive**......to design smaller components which yield well and combine them into the larger unit. This is a fundamental tenet of modern IC fabrication which “pure” SoC ignores.
Alpine’s MicroBoard substrate enables higher speed and density than SoC, with design time similar to PCB.

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<th>PCB</th>
<th>MicroBoard</th>
<th>SoC</th>
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<tbody>
<tr>
<td><strong>Performance</strong></td>
<td>1</td>
<td>100</td>
<td>10</td>
</tr>
<tr>
<td><strong>Complexity / $</strong></td>
<td>1</td>
<td>50</td>
<td>10</td>
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<tr>
<td><strong>Design Time</strong></td>
<td>1</td>
<td>1 - 2</td>
<td>10</td>
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Alpine’s SiP solution solves the cost and complexity limitations of traditional multi-chip approaches.

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<tr>
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<th>MCM/L</th>
<th>Alpine SiP</th>
<th>MCM/C</th>
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<tbody>
<tr>
<td><strong>Performance</strong></td>
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<td>40</td>
<td>10</td>
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<tr>
<td><strong>Interconnect Density</strong></td>
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<td>2</td>
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<tr>
<td><strong>Known Good Die</strong></td>
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<td>no</td>
<td>yes</td>
</tr>
<tr>
<td><strong>Design Time</strong></td>
<td>1</td>
<td>1 - 2</td>
<td>5</td>
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System complexity is growing at a greater rate than SoC and PCB based solutions – SiP solves this issue.
The microelectronics packaging industry is migrating towards more complex packages in order to satisfy the size and performance needs of the IC industry.

The Semiconductor Industry *must* provide the solution, but single-chip-integration alone is not enough.

In next generation designs we will achieve the optimum cost/benefit by using the best technology for each part of the system ......

*System in Package*