Emerging Memories

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Sponsors and Collaborators

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Non-Volatile Memory Technology Research Initiative (NMTRI) at Stanford University
Outline

- Opportunities for emerging memories
- Phase change memory
- Resistance change MIM memory
  - Metal oxide
  - Nano Conductive Bridge
  - Organic polymer, molecules
- Beyond the memory cell
What Technology Enabled the iPod Nano?

Source: Apple Computer, Inc.
Memory In Your Hands (~2010)

More than 400GB...

Wearable Gadget (20GB)
Pocket PC & USB (50GB)

IBS watch (Information Bank System) (100GB)
MPX Player (80GB)
Pet Robot (100GB)

Phone, Data, GPS, Game, Entertainment, ...

Memory Market: DRAM and Flash Dominate

Source: Gary Bronner (Rambus), Stanford EE 309 lecture, Fall 2007.
NAND Circa 2004 – 2005

- Multi-level cell (MLC)
- Density getting close to hard disk drive (HDD)

Areal Density (Gb/sq.in.)

- 1980
- 1990
- 2000
- 2010

- 230 Gb/in² demo
- 100% / yr
- 60% / yr
- 30% / yr
- GMR head
- Standard FF
- PRML channel
- Thin film disk
- IBM / Hitachi, highest AD products
- Competitors, mobile


DRAM and Flash Price Outlook

Ref: IDC + iSuppli

DRAM - 25%/year price decrease
further price drop with 6F² transition

Flash - rapid decline in price 2004 - 2007
followed by similar price decline as DRAM - ~ 25%/year

Note: Flash price assumes 2 bit/cell

Source: Gary Bronner (Rambus), Stanford EE 309 lecture, Fall 2007.
Memory Outlook (5 Years)

- Memory dominated by DRAM and Flash
- DRAM traditionally highest volume and lowest cost
- NAND Flash now cheaper than DRAM
  - Fundamental change
- No road blocks to scaling both to the year 2012
- Performance difference means NAND Flash goes after different applications
  - But low Flash prices mean it will expand rapidly

Source: Gary Bronner (Rambus), Stanford EE 309 lecture, Fall 2007.
Memory Materials

- What is required of a memory material between that sandwich of bit-line and word-line?

- To make a memory, all you need is a hysteresis loop!
  - Easy to claim memory effect
  - Difficult to satisfy memory requirements!

Example: Voltage bias induced resistance change (bi-directional programming)
Some Hysteretic Properties

- Charge storage in trap sites (charge, potential)
- Charge storage in capacitor (charge, potential)
- Phase change (resistance)
- Metal oxide (resistance)
- Nano filament formation (resistance)
- Ferroelectrics (electric dipoles)
- Magnetoresistance (resistance)
- Magnetic tunnel junction (resistance)
- Stiction force (resistance)
- Mechanical deformation (resistance)
- ...
### Table ERD3: Current Baseline and Prototypical Memory Technologies

<table>
<thead>
<tr>
<th>Storage Mechanism</th>
<th>Baseline Technologies</th>
<th>Prototypical Technologies [A]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DRAM</td>
<td>Floating Gate [E]</td>
</tr>
<tr>
<td></td>
<td>Standard [A]</td>
<td>Embedded [C]</td>
</tr>
<tr>
<td><strong>Cell Elements</strong></td>
<td><strong>2007</strong></td>
<td><strong>2008</strong></td>
</tr>
<tr>
<td><strong>Feature Size F, nm</strong></td>
<td><strong>6T</strong></td>
<td><strong>6T</strong></td>
</tr>
<tr>
<td><strong>Cell Area</strong></td>
<td><strong>6T</strong></td>
<td><strong>6T</strong></td>
</tr>
<tr>
<td><strong>Read Time</strong></td>
<td><strong>&lt;10 ns</strong></td>
<td><strong>&lt;10 ns</strong></td>
</tr>
<tr>
<td><strong>Write Time</strong></td>
<td><strong>&lt;10 ns</strong></td>
<td><strong>&lt;10 ns</strong></td>
</tr>
<tr>
<td><strong>Retention Time</strong></td>
<td><strong>&gt;10 y</strong></td>
<td><strong>&gt;10 y</strong></td>
</tr>
<tr>
<td><strong>Write Cycles</strong></td>
<td><strong>&gt;3E16</strong></td>
<td><strong>&gt;3E16</strong></td>
</tr>
<tr>
<td><strong>Write Operating Voltage (V)</strong></td>
<td><strong>2.5</strong></td>
<td><strong>2.5</strong></td>
</tr>
<tr>
<td><strong>Read Operating Voltage (V)</strong></td>
<td><strong>2</strong></td>
<td><strong>2</strong></td>
</tr>
<tr>
<td><strong>Write Energy (kJ/bit)</strong></td>
<td><strong>&gt;1E-15</strong></td>
<td><strong>&gt;1E-15</strong></td>
</tr>
<tr>
<td><strong>Comments</strong></td>
<td>Multiple-bit potential</td>
<td>Multiple-bit potential</td>
</tr>
<tr>
<td>Table ERD4</td>
<td>Transition Table for Emerging Research Memory Devices</td>
<td></td>
</tr>
<tr>
<td>------------</td>
<td>-------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN/OUT (Table ERD3)</td>
<td>Reason for IN/OUT</td>
</tr>
<tr>
<td>Nanofloating Gate Memory</td>
<td>OUT</td>
<td>Natural evolution of FG FLASH, No major research issues, Became a prototypical technology</td>
</tr>
<tr>
<td>Insulator Resistance Change Memory</td>
<td>OUT</td>
<td>Replaced by three new memory categories (see immediately below)</td>
</tr>
<tr>
<td>Fuse/Antifuse Memory</td>
<td>IN</td>
<td>Replacement for the Insulator Resistance Change memory</td>
</tr>
<tr>
<td>Ionic Memory</td>
<td>IN</td>
<td>Replacement for the Insulator Resistance Change memory</td>
</tr>
<tr>
<td>Electronic Effects Memory</td>
<td>IN</td>
<td>Replacement for the Insulator Resistance Change memory</td>
</tr>
<tr>
<td>Nanomechanical Memory</td>
<td>IN</td>
<td>New device concept, promising characteristics, several recent publications</td>
</tr>
</tbody>
</table>

Resistivity Switching

- For a memory device that relies on a change in the resistivity of the memory cell, we need a mechanism by which the resistance of the cell (material) is changed by an electrical input.

- This generally involves a change in the properties of the material in response to an electrical input.
  - Atomic arrangement leading to conductivity changes.

- What are the possible electrical inputs?
  - $I, B, V, E, Q=I*t, P=I*V, E=I*V*t$
Physics of Resistivity Switching

- The physics of resistivity switching for many newly “discovered” memory devices is not clearly known

- Often, application of a voltage or a current will induce resistivity switching

- But it is not clear whether the driving force is current, voltage, fluence, power, energy, or a combination of these

  - Often, the physics of switching is murky and mis-interpreted – need to be VERY careful when interpreting results and/or claims
Comparisons With Floating Gate

- **Phase Change Memory**
  - Non-volatile
  - Bit-alterable
  - Uni-directional programming
  - Can be re-written without first erasing
    - Low voltage programming
    - Higher endurance
  - Works more like an SRAM
    - But much slower read/write

### Table: Comparisons with Floating Gate

<table>
<thead>
<tr>
<th></th>
<th>Floating Gate [E]</th>
<th>PCM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NOR</td>
<td>NAND</td>
</tr>
<tr>
<td><strong>Storage Mechanism</strong></td>
<td>Charge on floating gate</td>
<td></td>
</tr>
<tr>
<td><strong>Cell Elements</strong></td>
<td>1T</td>
<td>1TIR</td>
</tr>
<tr>
<td><strong>Feature size F, nm</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td>2022</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td><strong>Cell Area</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>10 F^2</td>
<td>5 F^2</td>
</tr>
<tr>
<td>2022</td>
<td>10 F^2</td>
<td>5 F^2</td>
</tr>
<tr>
<td><strong>Read Time</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>10 ns</td>
<td>50 ns</td>
</tr>
<tr>
<td>2022</td>
<td>2 ns</td>
<td>10 ns</td>
</tr>
<tr>
<td><strong>W/E Time</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>1 µs/10 ns</td>
<td>1/0.1 ms</td>
</tr>
<tr>
<td>2022</td>
<td>1 µs/10 ns</td>
<td>1 ms/0.1 ms</td>
</tr>
<tr>
<td><strong>Retention Time</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>&gt;10 y</td>
<td>&gt;10 y</td>
</tr>
<tr>
<td>2022</td>
<td>&gt;10 y</td>
<td>&gt;10 y</td>
</tr>
<tr>
<td><strong>Write Cycles</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>&gt;1E5</td>
<td>&gt;1E5</td>
</tr>
<tr>
<td>2022</td>
<td>&gt;1E5</td>
<td>&gt;1E5</td>
</tr>
<tr>
<td><strong>Write Operating Voltage (V)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>2022</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td><strong>Read Operating Voltage (V)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>2022</td>
<td>1.1</td>
<td>1.1</td>
</tr>
<tr>
<td><strong>Write Energy (J/bit)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comments</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2005 ITRS: [http://public.itrs.net](http://public.itrs.net)
Phase Change Materials

- Same class of materials as the recording media of CD-RW and DVD-RW

- For DVD, a laser is used to write/erase by heating the GST
  - High energy -> amorphous, low energy -> crystalline
  - Volume changes upon crystallization/amorphization changes the light scattered from the lower energy reading laser

- For electrical phase change memory, the resistivity through the material is sensed by an external circuit
Phase Change Memory

**Operation Principle:** Device operates by switching between *low resistance* SET state and *high resistance* RESET state.

Electrical current pulses lead to intense localized heating (~$10^{11}$K/s) in the phase change layer.

Controlled pulses cause transition between the high resistivity amorphous phase and low resistivity crystalline phase.
Typical Phase Change Memory Device Structure

PCM – SET to RESET

PCM – RESET to SET

Electronic switching is the key to phase change memory device operation.

Programming

- Switch from crystalline state to amorphous state: < 10 ns
- Switch from amorphous state to crystalline state: ~ 50 ns
  - Requires nucleation and crystallization
- Thermal time constant: ~ a few nsec
- Programming is faster than most other “emerging memories” (e.g. metal oxide, nanoconductive bridge), but SET and RESET are asymmetric
Experimental Phase Change Memory Cells

Resistance, Current, Temperature

- **R, I, T** are all inter-related
- **Key issue:** large reset current

![Graph showing I-V curves and temperature changes](image)

**Figure 3:** Experimental and simulated I-V curves and simulated maximum temperature in the GST. The chalcogenide should start to melt at about 0.4 mA.

**Programming pulse = 100 ns (with varying amplitude)**

**Figure 4:** Experimental programming curve corresponding to the electrical characteristic in Fig.3. The two curves refer to the same bit in the SET and in the RESET state. Note that the resistance starts to increase for a current of the order of 0.4-0.5 mA.

Programming Current

- **One of the main problems of PCM is the large programming current**
  - Larger (device width) access transistor → cell area larger
  - Higher power consumption

- **Programming current should scale down with memory cell size (transistor gate width)**

Reset Current Reduction

- Reducing reset current is one of the most important issues of phase change memory
  - Reduce contact area (brute force)
  - Engineer the device structure to achieve highest heating for a certain current
  - Engineer the interface thermal and electrical resistance of the GST / electrode interface
  - Engineer the electrical and thermal properties of the phase change material
Reset Current Reduction Needed

- Typical high performance transistor drive current
  \( \sim 1 \text{mA/\mu m} \)

- At 32 nm, for \( W/L=4 \), \( I=128 \mu A \)

\[ I_{\text{RESET}} = 128 \mu A \]

Diameter = 18 nm
(S. Lai et al.)

Novel Cell Structure To Reduce Contact Area

Y.H. Ha et al., “An Edge Contact Type Cell for Phase Change RAM Feature in Very Low Power Consumptions,” Symp. VLSI Tech., paper 12B-4, 200
Thermal Engineering of Cell Structure

- Engineer the heated area to confine the heat

Common PCM Device Structures

Pore and lance structure

\[\text{H. Horii et al., VLSI Symp. on Tech. 2003}\]

\[\text{μtrench structure}\]

\[\text{F. Pellizzer et al., VLSI Symp. on Tech. 2004}\]

Planar structure

\[\text{M.Lankhorst et al., Nature Material, April 2005}\]

As device size is scaled down, the temperature distribution away from the cell is the same when normalized to the radial size of the cell.

- Select transistor provides the set/reset current
- Because high reset current required (100’s of uA), select transistor is larger than minimum width

Array Configurations (BJT, Diode)

- Parasitic transistor (pnp) transistor is formed using “standard” CMOS
- Needs special process in CMOS to implement this diode (extra cost!)
- WL carries substantial current, therefore WL (in addition to BL) must be designed to handle current
  - Sub-divide columns to handle current (IR drop)

---

## PCM Development Status

<table>
<thead>
<tr>
<th>Company</th>
<th>Intel</th>
<th>Samsung</th>
<th>STMicroelectronix</th>
<th>IBM/Infineon/Macronix</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Source</strong></td>
<td>ISSCC’02</td>
<td>ISSCC’04</td>
<td>VLSI’05</td>
<td>VLSI’04</td>
</tr>
<tr>
<td><strong>Technology Node [nm]</strong></td>
<td>180</td>
<td>180</td>
<td>120</td>
<td>180</td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>4Mb</td>
<td>64Mb</td>
<td>256Mb</td>
<td>4Mb/8Mb</td>
</tr>
<tr>
<td><strong>Cell size [μm²-F²]</strong></td>
<td>0.25-7.7</td>
<td>0.5-16</td>
<td>0.16-16</td>
<td>1.3-40/0.32-10</td>
</tr>
<tr>
<td><strong>Material</strong></td>
<td>GST</td>
<td>GST</td>
<td>N-doped GST</td>
<td>GST</td>
</tr>
<tr>
<td><strong>Cell type</strong></td>
<td>Pore</td>
<td>Lance</td>
<td>Ring</td>
<td>μTrench</td>
</tr>
<tr>
<td><strong>Selector type</strong></td>
<td>Diode</td>
<td>MOSFET</td>
<td>Tri-MOSFET</td>
<td>MOSFET/BJT</td>
</tr>
<tr>
<td><strong>Current/bit [mA]</strong></td>
<td>1</td>
<td>2</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td><strong>Operation voltage [V]</strong></td>
<td>3.3</td>
<td>3.0</td>
<td>3.0</td>
<td>3.3</td>
</tr>
<tr>
<td><strong>Write time [ns]</strong></td>
<td>100</td>
<td>120</td>
<td>-</td>
<td>150</td>
</tr>
<tr>
<td><strong>Endurance [cycles]</strong></td>
<td>$10^8$</td>
<td>-</td>
<td>$10^9$</td>
<td>$10^{11}$</td>
</tr>
</tbody>
</table>

Biggest Question for all memories:

Scalability
Multi-Bit Phase Change Memory

- Write and verify (similar to FLASH)
- Tune slope of falling pulse edge
- Key: control bit-cell distribution

Bridge Cell – Scaling to 60 nm²

- In conventional structures, cross-sectional area scales with CD²
- In Phase-Change Bridge, cross-sectional area scales with
  - W * H (film thickness)
  - H can be scaled independent of lithographic CD

CD = Critical Dimension

<table>
<thead>
<tr>
<th>Storage Mechanism</th>
<th>Nanomechanical Memory</th>
<th>Fuse/Antifuse Memory</th>
<th>Ionic Memory</th>
<th>Electronic Effects Memory</th>
<th>Macromolecular Memory</th>
<th>Molecular Memories</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Electrostatically</td>
<td>Multiple mechanisms</td>
<td>Ion transport</td>
<td>Multiple mechanisms</td>
<td>Multiple mechanisms</td>
<td>Not known</td>
</tr>
<tr>
<td></td>
<td>controlled mechanical</td>
<td></td>
<td>and redox reaction</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cell Elements</td>
<td>1T1R or 1D1R</td>
<td>1T1R or 1D1R</td>
<td>1T1R or 1D1R</td>
<td>1T1R or 1D1R</td>
<td>1T1R or 1D1R</td>
<td>1T1R or 1D1R</td>
</tr>
<tr>
<td>Device Types</td>
<td>1) nanobridge/</td>
<td>M-I-M (e.g., Pt/</td>
<td>1) cation migration</td>
<td>1) Charge trapping</td>
<td>M-I-M (nc)</td>
<td>Bi-stable switch</td>
</tr>
<tr>
<td></td>
<td>cantilever</td>
<td>NiO/Pt)</td>
<td>2) anion migration</td>
<td>2) Mott transition</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2) telescoping CNT</td>
<td></td>
<td>3) Nanoparticle</td>
<td>3) FE barrier effects</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Feature size F</td>
<td>Min. required</td>
<td>~65 nm</td>
<td>~65 nm</td>
<td>~65 nm</td>
<td>~65 nm</td>
<td>~65 nm</td>
</tr>
<tr>
<td></td>
<td>Best projected</td>
<td>~65 nm</td>
<td>~65 nm</td>
<td>~65 nm</td>
<td>~65 nm</td>
<td>~65 nm</td>
</tr>
<tr>
<td>Cell Area</td>
<td>Min. required</td>
<td>$10^6$ F</td>
<td>$10^5$ F</td>
<td>$10^5$ F</td>
<td>$10^5$ F</td>
<td>$10^5$ F</td>
</tr>
<tr>
<td></td>
<td>Best projected</td>
<td>$8.5^6$ F</td>
<td>$8.5^5$ F</td>
<td>$8.5^5$ F</td>
<td>$8.5^5$ F</td>
<td>$8.5^5$ F</td>
</tr>
<tr>
<td></td>
<td>Demonstrated</td>
<td>Data not available</td>
<td>Data not available</td>
<td>Data not available</td>
<td>Data not available</td>
<td>Data not available</td>
</tr>
<tr>
<td>Read Time</td>
<td>Min. required</td>
<td>&lt;15 ns</td>
<td>&lt;15 ns</td>
<td>&lt;15 ns</td>
<td>&lt;15 ns</td>
<td>&lt;15 ns</td>
</tr>
<tr>
<td></td>
<td>Best projected</td>
<td>&lt;15 ns</td>
<td>&lt;15 ns</td>
<td>&lt;15 ns</td>
<td>&lt;15 ns</td>
<td>&lt;15 ns</td>
</tr>
<tr>
<td></td>
<td>Demonstrated</td>
<td>~50 ns [G]</td>
<td>Data not available</td>
<td>Data not available</td>
<td>Data not available</td>
<td>Data not available</td>
</tr>
<tr>
<td>Write Cycles</td>
<td>Min. required</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
</tr>
<tr>
<td></td>
<td>Best projected</td>
<td>~10 y</td>
<td>~10 y</td>
<td>~10 y</td>
<td>~10 y</td>
<td>~10 y</td>
</tr>
<tr>
<td></td>
<td>Demonstrated</td>
<td>~10 y</td>
<td>~10 y</td>
<td>~10 y</td>
<td>~10 y</td>
<td>~10 y</td>
</tr>
<tr>
<td>Write operating voltage (V)</td>
<td>Min. required</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
</tr>
<tr>
<td></td>
<td>Best projected</td>
<td>0.5 V</td>
<td>0.5 V</td>
<td>&lt;3 V</td>
<td>&lt;3 V</td>
<td>80 mV [V]</td>
</tr>
<tr>
<td></td>
<td>Demonstrated</td>
<td>1.5 V [A]</td>
<td>0.5 V [E]</td>
<td>0.6-0.7 V [G]</td>
<td>3-5 V [LM]</td>
<td>~2 V [S]</td>
</tr>
<tr>
<td>Read operating voltage (V)</td>
<td>Min. required</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td>Best projected</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td>Demonstrated</td>
<td>1.3 V [A]</td>
<td>0.4 V [E]</td>
<td>0.7 V [L]</td>
<td>1 V [S]</td>
<td>0.5 V [W]</td>
</tr>
<tr>
<td>Write energy (J/bit)</td>
<td>Min. required</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
</tr>
<tr>
<td></td>
<td>Best projected</td>
<td>Not known</td>
<td>Not known</td>
<td>1E-15 [J]</td>
<td>1E-10</td>
<td>2E-19 [Y]</td>
</tr>
<tr>
<td></td>
<td>Demonstrated</td>
<td>Data not available</td>
<td>Data not available</td>
<td>Data not available</td>
<td>Data not available</td>
<td>Data not available</td>
</tr>
<tr>
<td>Comments</td>
<td>Inverse voltage scaling presents a problem</td>
<td>Potential for multi-bit storage</td>
<td>Potential for multi-bit storage</td>
<td>Low read voltage presents a problem</td>
<td>Potential for multi-bit storage</td>
<td>160 Kbit prototype chip demonstrated [V]</td>
</tr>
<tr>
<td>Research activity [Z]</td>
<td>22</td>
<td>30</td>
<td>47</td>
<td>44</td>
<td>77</td>
<td>90</td>
</tr>
</tbody>
</table>
### Comparisons

- Metal oxide and ionic (nano-conductive bridge) memory are more “mature” (compared to polymer memory and molecular memory).

- A significant gap exists between “projected” and “demonstrated” characteristics – opportunities for more research.

#### Table: Memory Comparison

<table>
<thead>
<tr>
<th></th>
<th>Metal Oxide</th>
<th>Ionic Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Storage Mechanism</strong></td>
<td>Charge on floating gate</td>
<td>Reversibly changing amorphous and crystalline phases</td>
</tr>
<tr>
<td><strong>Cell Elements</strong></td>
<td>1T</td>
<td>1TIR</td>
</tr>
<tr>
<td><strong>Feature size F, nm</strong></td>
<td>2007 90</td>
<td>2007 90</td>
</tr>
<tr>
<td></td>
<td>2022 18</td>
<td>2022 18</td>
</tr>
<tr>
<td><strong>Cell Area</strong></td>
<td>2007 10 F²</td>
<td>2007 10 F²</td>
</tr>
<tr>
<td></td>
<td>2022 10 F²</td>
<td>2022 10 F²</td>
</tr>
<tr>
<td><strong>Read Time</strong></td>
<td>2007 10 ns</td>
<td>2007 10 ns</td>
</tr>
<tr>
<td></td>
<td>2022 2 ns</td>
<td>2022 2 ns</td>
</tr>
<tr>
<td><strong>W/E Time</strong></td>
<td>2007 1 µs/10 ms</td>
<td>1 µs/10 ms</td>
</tr>
<tr>
<td></td>
<td>2022 1 µs/10 ms</td>
<td>1 µs/10 ms</td>
</tr>
<tr>
<td><strong>Retention Time</strong></td>
<td>2007 &gt;10 y</td>
<td>2007 &gt;10 y</td>
</tr>
<tr>
<td></td>
<td>2022 &gt;10 y</td>
<td>2022 &gt;10 y</td>
</tr>
<tr>
<td><strong>Write Cycles</strong></td>
<td>2007 &gt;1E5</td>
<td>2007 &gt;1E5</td>
</tr>
<tr>
<td></td>
<td>2022 &gt;E15</td>
<td>2022 &gt;E15</td>
</tr>
<tr>
<td><strong>Write Operating Voltage (V)</strong></td>
<td>2007 12</td>
<td>2007 12</td>
</tr>
<tr>
<td></td>
<td>2022 12</td>
<td>2022 12</td>
</tr>
<tr>
<td><strong>Read Operating Voltage (V)</strong></td>
<td>2007 2</td>
<td>2007 2</td>
</tr>
<tr>
<td></td>
<td>2022 1.1</td>
<td>2022 1.1</td>
</tr>
<tr>
<td></td>
<td>2022 &gt;1E-15 [F]</td>
<td>2022 &gt;1E-15 [F]</td>
</tr>
</tbody>
</table>

#### Notes:
- **2007 ITRS:** http://www.itrs.net
- **Device Types:**
  - Memory: Multiple mechanisms
  - Ion transport and redox reaction
- **Feature Size F:**
  - Min. required: <65 nm
  - Best projected: >10 nm

#### Department of Electrical Engineering

2008.04.03

H.-S. Philip Wong
Resistive Switching M-I-M Structures

Typical Resistance Memory Switching

- Metal/oxide/metal (M-I-M) device structure
- Metals are typically noble metal (e.g. Pt)

Bistable: memory effect

Monostable: no memory effect

Metal Oxide M-I-M Memory

**Motivation:**
- Low programming voltage (< 3V)
- Low programming current
- Uni-directional programming
  - Easier to build cross-point array
- Material set compatible with conventional semiconductor processing (e.g. Ni)

**Key issues:**
- Physics of resistive switching
- Device scaling properties
Key Features: Metal Oxide M-I-M Memory

- Memory switching observed in many metal oxides
  - NiO$_x$, TiO$_x$, Nb$_2$O$_5$, Al$_2$O$_3$, Ta$_2$O$_5$, CuO$_x$, WO$_x$, CoO
  - Cr doped perovskite oxides: SrZrO$_3$, (Ba,Sr)TiO$_3$, SrTiO$_3$
  - Cu doped MoO$_x$, Al$_2$O$_3$, ZrO$_2$, Al doped ZnO
  - Pr$_{0.7}$Ca$_{0.3}$MnO$_3$ (PCMO)

- Physical mechanisms are not clearly understood
  - Migrating ions? Vacancies? Role of the electrode?

- Generally attributed to formation of conductive filaments between the metal electrodes
  - On-state resistance should not depend on device area
  - Off-state resistance should be area dependent
NiO

- NiO is one of the most studied systems
- Reset to high resistance state (HRS)
- Set to low resistance state (LRS)

![Graph showing voltage and current levels](image)

**Fig. 4** Voltage and current levels of test programming pulses. Pulse width is on the order of ns for forming, read and set, and is on the order of μs for reset.


Source: S. Seo (2006)
LRS $\rightarrow$ HRS and HRS $\rightarrow$ LRS Transition

- HRS $\rightarrow$ LRS transition
  - Filament generation
- LRS $\rightarrow$ HRS transition
  - Filament rupture

LHS Correlated with Compliance Current

- Large compliance → low resistance
  - Thicker filament?

\[ \text{current (mA)} \]

\[ \text{voltage (V)} \]

\[ V_{off} \rightarrow V_{on} \]

\[ I_{\text{max for } 40mA} \]

\[ I_{\text{max for } 25mA} \]

\[ 40mA \]

\[ 25mA \]

\[ \text{TiO}_2 \]

\[ \text{NiO} \]


Retention and Endurance Cycles

Cell size = 0.3 µm x 0.7 µm

Bipolar Switching – Cr: SrZrO3 and Cr: SrTiO3

- \( \text{Cr}^{3+} \rightarrow \text{Cr}^{4+} + \text{e}^- \)


Metal Oxide Switching Mechanisms

Many models proposed

- Migration of anions toward anode (or mobile oxygen vacancy toward cathode) (e.g. in TiO$_2$)
- Transition metal valence states (e.g. Cr$^{n+}$ in SrTiO$_3$)
- Ni vacancy (in NiO)
- Charge trap in defect sites
- Metal insulator transition (Mott transition)

**Mechanism for each material is different**

Evidence of Filamentary Conduction

NiO Memory

- 3V program
- Direct over-write
- $10^6$ cycles

Main issues:

- 2 mA programming current
- 10 ns HRS $\rightarrow$ LRS, 5$\mu$s (or multiple 100ns) LRS $\rightarrow$ HRS

Nano Conductive Bridge Memory

1. Redox reaction
2. Ion migration (cation toward cathode)

Key Features: Ionic M-I-M Memory

- Many solid electrolyte have been used
  - Ag/Ag$_2$S, Ag-Ge-Se, Ag-Ge-S, Cu-WO$_3$, Cu/Cu$_2$S, Cu/Ta$_2$O$_5$, Ag/Zn$_x$Cd$_{1-x}$S, Cu/Zn$_x$Cd$_{1-x}$S, Zn/Zn$_x$Cd$_{1-x}$S

- One of the electrodes:
  - Easily oxidizable metal, e.g. Ag$^+$ in Ag$_2$S, Cu$^+$ in Cu$_2$S or
  - Compounds with high solubility of the redox active cation e.g. Ag$^+$ in GeSe$_x$

- Fast cation diffusion desired

- Generally attributed to formation of conductive filaments between the metal electrodes
  - On-state resistance should not depend on device area
  - Off-state resistance should be area dependent
Nanoconductive Bridge Typical I-V Characteristics

- Bipolar, asymmetric programming/erase
- Low programming/erase voltage
- Forming required

- Ag top electrode (active electrode)
- GeSe chalcogenide glass as solid electrolyte
- W bottom electrode (inert electrode)

Device Size Dependence

- $R_{\text{ON}}$ independent of area
- $R_{\text{OFF}}$ increases with decreasing area
- Consistent with filamentary conduction model

Multi-bit Possibility

- ON-state resistance is a function of programming current

![Graph showing the relationship between ON-resistance and program current limit.]

Fig. 6: CBRAM multi-level capability, programming currents for ON-levels 1: 0.5μA, 2: 2μA, and 3: 20μA, respectively (via diameter 100nm).

Cu/Cu$_2$S NanoConductive Bridge

- Nanoscale electroplating
- Forming and dissolution of metallic filaments

- 30 nm diameter


**Ag/Ag$_2$S/Pt**

An oxidizable electrode (Ag, Cu etc.) is needed to fulfill the forming and dissolving filamentary conduction paths.


Switching at (± 0.6 V, 1 MHz)

- **Top:** As-formed switched-on state
- **Middle:** Switched-off state
- **Bottom:** Switched-on state after the initial switching-off process (bottom).
Evidence of Filamentary Conduction

Cu:MoO\textsubscript{x}

NanoConductive Bridge

**Motivation:**
- On/Off ratio improves with scaling down.
- If the filament can be formed reproducibly, this class of devices may be scalable to atomic dimensions.

**Key issues:**
- Currently, switching voltage is too low (<0.5V)
- Programming speed
- Retention
- Bipolar switching voltage required
Molecular and Polymeric M-I-M Memories

Categories:

- Polymer
- Small molecule
- Donor-acceptor complexes
- Mobile ion
- Nanoparticle blended in organics

Switching mechanism largely unknown and hotly debated

### Organic M-I-M Memory

**Polymer**

<table>
<thead>
<tr>
<th>Switching type</th>
<th>Structure</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Hysteresis, without threshold or NDR</td>
<td>ITO / P60Me / Al</td>
<td>[39]</td>
</tr>
<tr>
<td>2. Reverse polarity switching, no NDR</td>
<td>AI / PSF / BaAl</td>
<td>[43]</td>
</tr>
<tr>
<td>3. Volatile or 4 WORM depending on conditions</td>
<td>ITO or Mo / PMMA, PS, PEMA or PMMA / graphite</td>
<td>[36]</td>
</tr>
<tr>
<td>5. Switching by either polarity, NDR</td>
<td>ITO / MEH-PPV / Al</td>
<td>[44]</td>
</tr>
</tbody>
</table>

**Mobile ion**

<table>
<thead>
<tr>
<th>Switching type</th>
<th>Structure</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Hysteresis, without threshold or NDR</td>
<td>PEDOT:PSS:NaCl / Gt-co-PEO / Al</td>
<td>[66]</td>
</tr>
<tr>
<td>2. Reverse polarity switching, no NDR</td>
<td>Pt / MEHPPV / RbAg514 /Ag</td>
<td>[67]</td>
</tr>
<tr>
<td></td>
<td>? / PPhA:NaCl / ?</td>
<td>[65]</td>
</tr>
</tbody>
</table>

**Donor-acceptor complexes**

<table>
<thead>
<tr>
<th>Switching type</th>
<th>Structure</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>2. Reverse polarity switching, no NDR</td>
<td>Cu / CuTCNQ / Al</td>
<td>[47]</td>
</tr>
<tr>
<td></td>
<td>ITO / EuVB-co-PVK / Al</td>
<td>[58]</td>
</tr>
<tr>
<td></td>
<td>ITO / PEDOT:PSS / Fe-complex:PVK / LiF / Ca /Ag</td>
<td>[56]</td>
</tr>
<tr>
<td></td>
<td>HOPG / NBMN / pDA / STM</td>
<td>[53]</td>
</tr>
<tr>
<td></td>
<td>Al / CuTCNQ / Al</td>
<td>[48]</td>
</tr>
<tr>
<td></td>
<td>Al / TTF-PCBM-PS</td>
<td>[54]</td>
</tr>
<tr>
<td></td>
<td>HOPG / CDHAB / STM-W</td>
<td>[98]</td>
</tr>
<tr>
<td></td>
<td>Cu / CuTCNQ / Cu</td>
<td>[50]</td>
</tr>
<tr>
<td></td>
<td>ITO / P3HT-CNT / Al</td>
<td>[76]</td>
</tr>
<tr>
<td></td>
<td>Cu / CuTCNQ / Al</td>
<td>[45]</td>
</tr>
</tbody>
</table>

### Small molecule

**Nanoparticle blend**

<table>
<thead>
<tr>
<th>Switching type</th>
<th>Structure</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Hysteresis, without threshold or NDR</td>
<td>AI / (Au2NT or B1):PS / Al</td>
<td>[74]</td>
</tr>
<tr>
<td>2. Reverse polarity switching, no NDR</td>
<td>Al / AIDCN / Al / AIDCN / Al</td>
<td>[68,69]</td>
</tr>
<tr>
<td>4. WORM</td>
<td>Al / AIDCN / Al / AIDCN / Al / AIDCN / Al</td>
<td>[71]</td>
</tr>
<tr>
<td></td>
<td>Ag / CNPF / Ag / CNPF / Ag</td>
<td>[80]</td>
</tr>
<tr>
<td></td>
<td>? / TDCN / Ag / TDCN / ?</td>
<td>[77]</td>
</tr>
<tr>
<td></td>
<td>Al / Alq3 / (Al) / Alq3 / Al</td>
<td>[62,70]</td>
</tr>
<tr>
<td></td>
<td>ITO / (Au-TPP)-xBPFB / Al</td>
<td>[41,42]</td>
</tr>
<tr>
<td></td>
<td>ITO / (Au-TPP)-xHTPA / Ca / Al</td>
<td>[41]</td>
</tr>
<tr>
<td></td>
<td>ITO / (Au-TPP)-xHTPA / Al</td>
<td>[41]</td>
</tr>
<tr>
<td></td>
<td>ITO / (Au-TPP)-xHTPA / xHTPA / Al</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Al / NPB / Al / NPB / Al</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Cu / Alq3 / (Al) / Alq3 / Al</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Cu / Alq3 / (Al) / Alq3 / Al</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Cu / Alq3 / (Al) / Alq3 / Al</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Ni / Alq3 / (Al) / Alq3 / Al</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Al / Alq3 / (Mg) / Alq3 / Al</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Al / Alq3 / (Alq3 / Alq3 / Alq3</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Al / Alq3 / (Alq3 / Alq3</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Al / Alq3 / (Alq3 / Alq3</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Al / Alq3 / (Cu) / Alq3 / Al</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Al / Alq3 / (CuPc) / Alq3 / Al</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td>Al / (Au-DT):P3HT / Al</td>
<td>[75]</td>
</tr>
</tbody>
</table>

Beyond The Memory Cell

- Cell selection device for cross-point memory
- Non-volatile memory enabled circuits
Recent Efforts – Cross-Point Memory

30 nm half-pitch cross-point memory

Cross-Point Memory Cell Selection Device

**Requirements:**

- Stackable, low temperature processing
- Enough current drive for programming
- Unidirectional and (ideally, bi-directional) programming
Silicon or Oxide Diode
- Uses NiO as p-type, TiO₂ as n-type semiconductor with $\phi 50\mu m$ ($\sim 10^{2}\text{A/cm}^2$)
- Process temperature $< 300\degree \text{C}$.
- Current density needs to be increased by a few orders for reasonably small OxRRAM cells.

Oxide diode property

Binary oxide switching

Switching combined with oxide diode

Source: S. Seo (2006)
Multi-Layer Cross-Point Memory

- Plug-BE structure. (diameter : 0.2um)
- Diode can be inserted in the plug position.
- 4x5 array cross-point structure

⇒ Cross point structure enables 4F² density.
(Effective cell area 2F²)
Even higher density is possible by stacking them.

Cross-Point Memory Array with Selective Nanowire Diode

Memory-Enabled Circuits

- Non-volatile SRAM
- Re-configuration switch
- Three-terminal logic switch (non-volatile)
Non-Volatile SRAM Using Nanoconductive Bridge

Fig. 3: Current flow during (a) STORE with BL=0 and BL B=1, (b) RESTORE, and (c) RESET.

Fig. 5: Cross-section schematic of the NVSRAM.

Fig. 6: Top view optical image of the test structure.

Low On-Resistance – Use As Reconfiguration Switch

<table>
<thead>
<tr>
<th>Feature</th>
<th>Nano-Bridge</th>
<th>MOSFET</th>
<th>Phase change</th>
<th>MEMS switch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>0.03 μm</td>
<td>1 μm</td>
<td>0.1 μm</td>
<td>1mm</td>
</tr>
<tr>
<td>ON resistance</td>
<td>50 Ω</td>
<td>1kΩ</td>
<td>1kΩ</td>
<td>&lt;1Ω</td>
</tr>
<tr>
<td>Switching Time</td>
<td>~100 μs</td>
<td>1ns</td>
<td>10ns</td>
<td>&gt;1 μs</td>
</tr>
<tr>
<td>Threshold Voltage</td>
<td>&lt;1V</td>
<td>&lt;2V</td>
<td>&lt;1V</td>
<td>&gt;20V</td>
</tr>
<tr>
<td>Cycling endurance</td>
<td>10^3-10^5</td>
<td>&gt;10^15</td>
<td>10^12</td>
<td>&lt;10^5</td>
</tr>
<tr>
<td>Non-volatility</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Nano Conductive Bridge (Three Terminal)

F : Concept of three terminal NanoBridge. When positive voltage is applied to control line, metal is precipitated between two metal wires via electro-chemical reactions. Negative voltage results in precipitated metal dissolving in solid electrolyte.

Conclusions

- **New materials enable new memory devices**
  - Plenty of new materials, difficult to satisfy memory requirements

- **Scalability is a key issue**
  - Stackable, small cell size, multi-bit/cell

- **New read / write / endurance characteristics enable new circuit/system design**

- **Future applications will be enabled by new memory technologies**