Optical Interconnects on Processors?
I Hate Predicting the Future

- The only guarantee is:
  - The future will happen, and you will be wrong

- So I will initially avoid saying WHETHER it will happen

- Focus instead on the issues that need to be solved

- And potential advantages and non-advantages
My Biggest Issue

- Is basically about packaging:
  - Need three surfaces
    - Power in
    - Heat Out
    - Light In/Out

- Light needs to travel through
  - Power, or heat sink

- Problem is not the vias
  - It is turning the corner
Signal Velocity for Repeated wires

- Under SIA scaling, pretty constant over many generations
- Under conservative scaling, slow change at sub-0.1µm techs
  - Makes wire delay increase slowly

![Graph showing signal velocity for repeated wires under SIA and conservative scaling across different feature sizes.]
Observations: On Chip Wires

• I feel sorry for the maligned VLSI wire
  – It really is not that bad
• If you scale the wires
  – You get more of them per mm
  – With repeaters the delay/mm scales slowly
    • Less than 1ns across a chip
  – Bandwidth per wire scales with technology
  – Total bandwidth/mm scales as $1/\alpha^2$
  – Delay across the chip is roughly constant in ps
• If you only need a few wires, $O(1000)$
  – You can make them thicker and wider
  – Velocity goes up
Observations: Off Chip Wires

• Behind each photonic device is an electronic link
  – Need to do data slicing, clock recovery on input
  – Need to drive VCSELs, or modulator
  – So speed/power is going to be limited by electronics
• Can make electrical links run at 10+Gb/s
  – Have demonstrations today
  – But have tremendous issues with loss in package and wire
    • Equalization works, but takes area and power

• So it seems like it comes down to packaging
  – Is optics easier to package than high quality package?
  – How far / how many connectors does the signal go through?