Nanoelectronics in Japan and TIA
Part 2 of 7

October 17 2013

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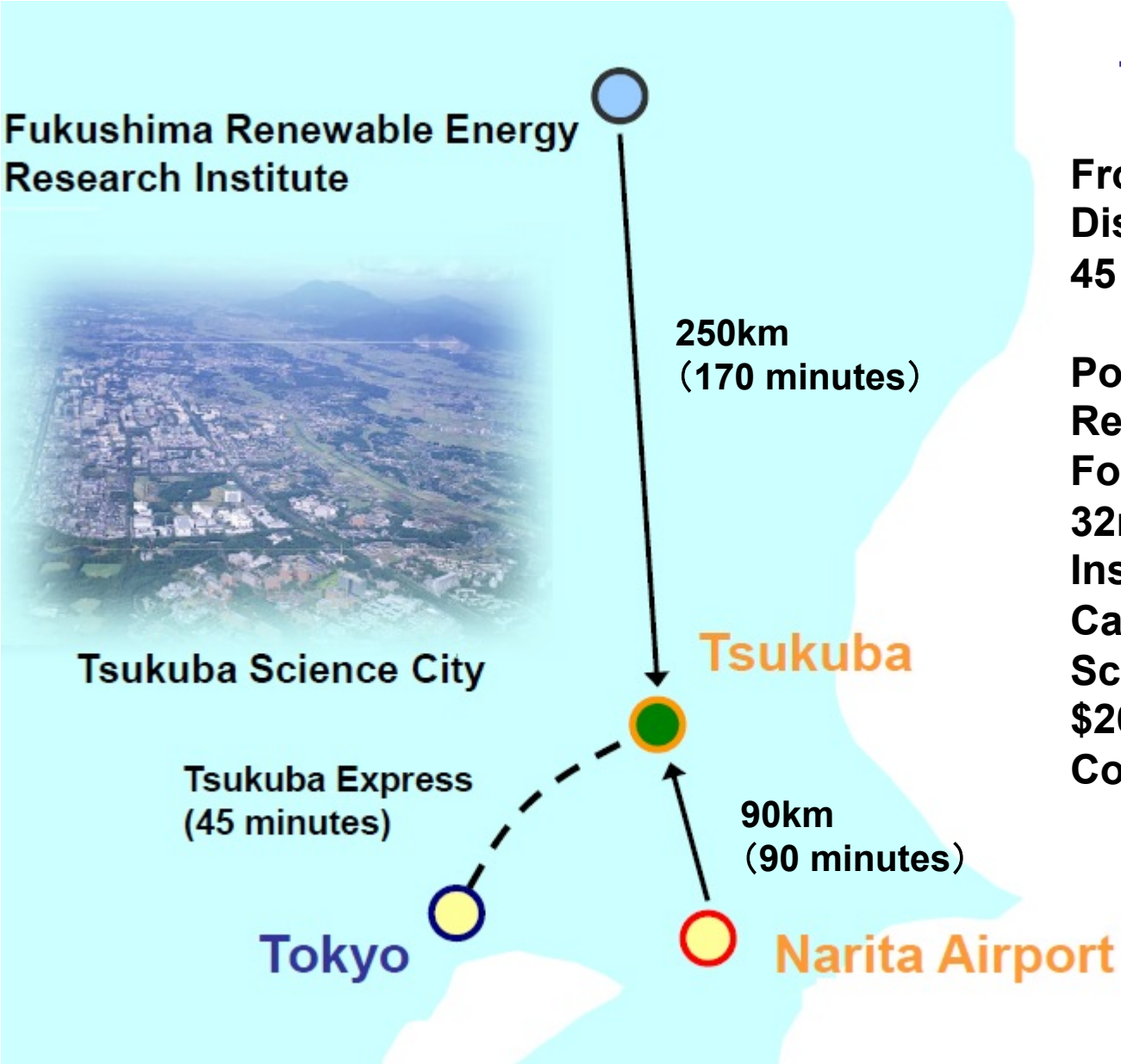
Tsukuba Science City



Tsukuba Science City

From Tokyo:
Distance 60km
45 minutes by Tsukuba Exp

Population:210,000
Researchers:20,000
Foreign residents:7,000
32national labs, 300research Institutions
Cabinet decision to create Science city 50 years ago.
$26billion invested for its Construction.

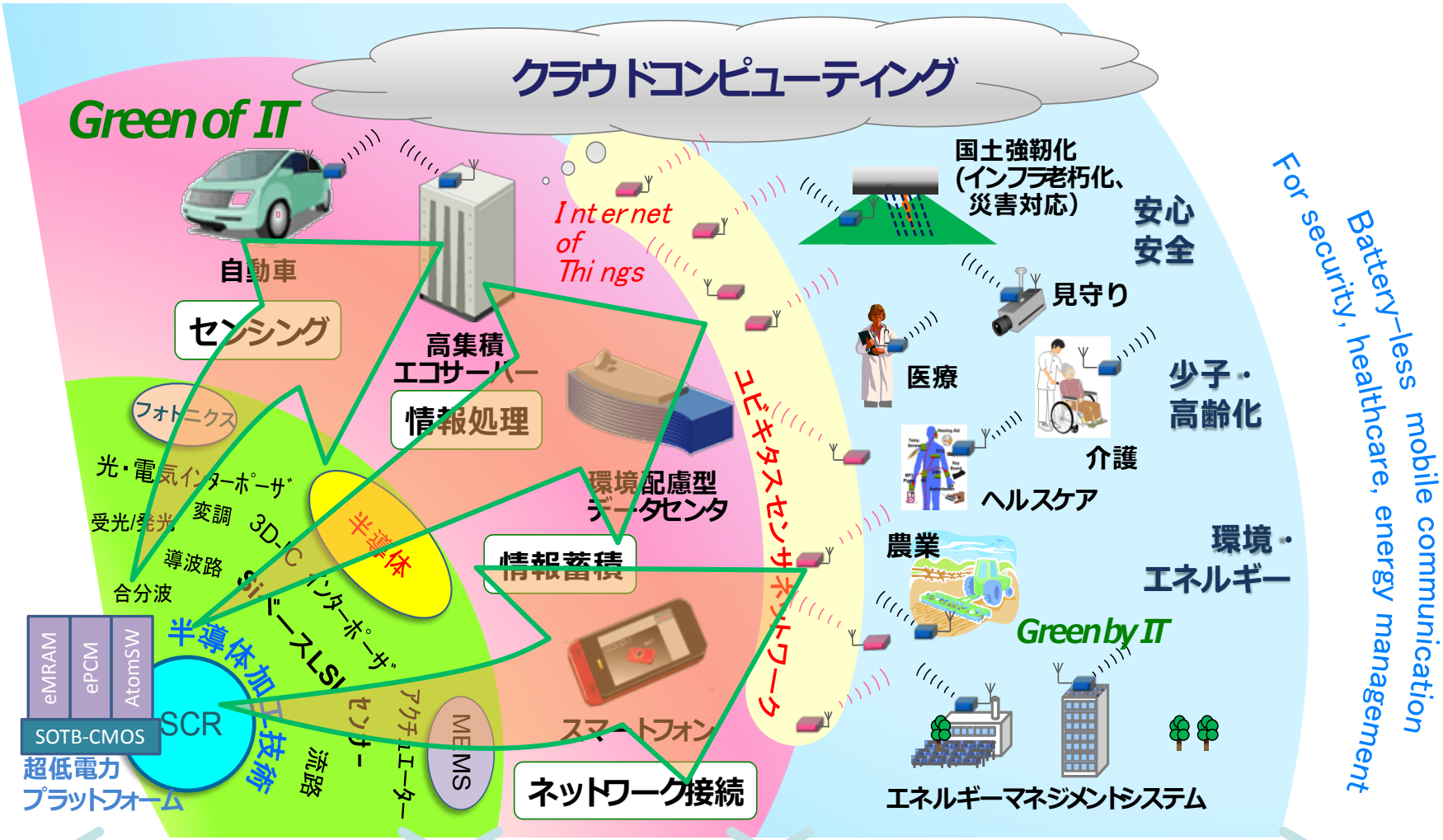
Facts & Figures of TIA-nano (Medium-Term Plan)

	2011FY	2012FY	Accumulation until 2012	Medium-Term Plan
Overall Project Scale (billion JPY)	13	25	76	100 billion JPY
Percentage of Public Funds (%)	88	85	-	70% or less
Number of Projects	23	26	26	>30
Number of Industrial Partners	93	119	128	>300
Number of Researchers and Students	529	832	-	>1,000
Number of TIA-Graduate Students	139	209	363	>500

# of Foreign Companies	5	7	
# of Foreign Researchers	60	49	
# of Papers	207	270	550
# of Applied Patents	139	228	386

TIA's vision of future society

•Super Low Power Technology:Basis for IOT(Internet of Things)

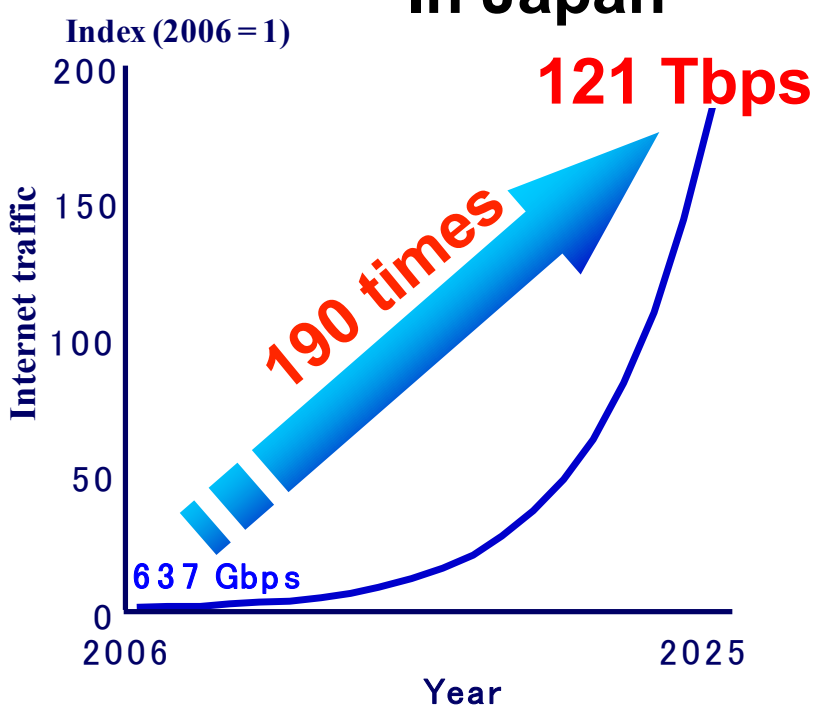


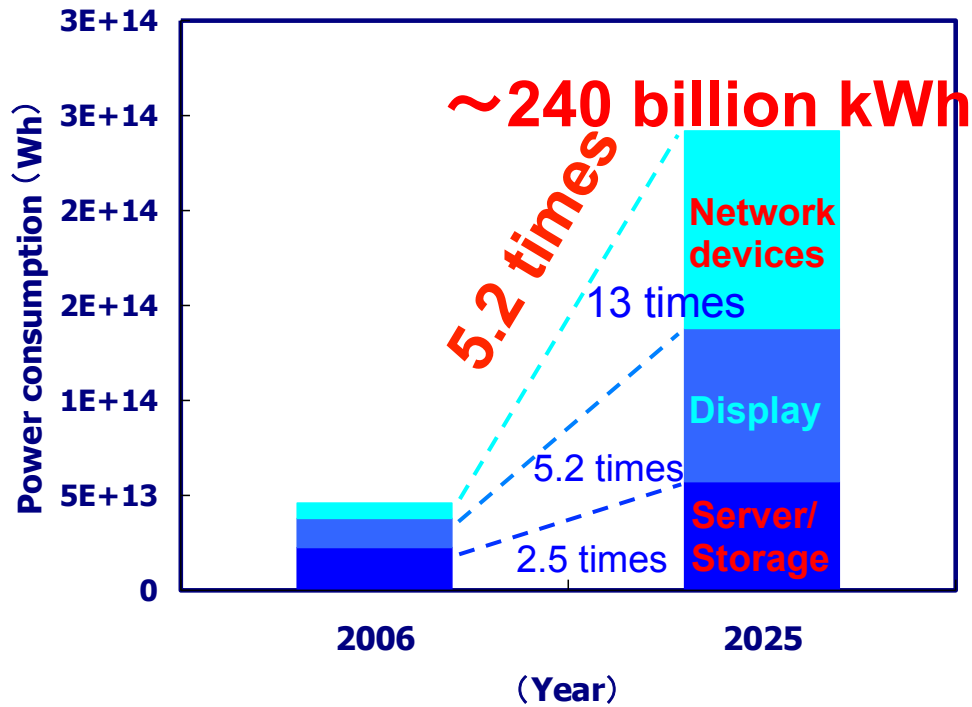
TIA R&D Current business Future industry

Increased Power Consumption of ICT

Green of ICT is required for sustainable ICT society.

In Japan





190 times increase in traffic

- 5.2 times increase
- ICT system will consume 20% of total domestic electric power generation

Source: Ministry of Economy, Trade and Industry, Japan

Key issues for Green Nanoelectronics tackled by 5+1 Projects

Key Issues

- ◆Dynamic power of logic circuits and memory
  - ➢Low-voltage operation
- ◆Stand-by power of logic circuits and memory
  - ➢Low voltage and low leakage
  - ➢Non-volatility and reconfigurability
- ◆Interconnects
  - ➢Low resistance materials
  - ➢Optical interconnect (Si photonics)

·FIRST, Green Nanoelectronics project Dr. Yokoyama

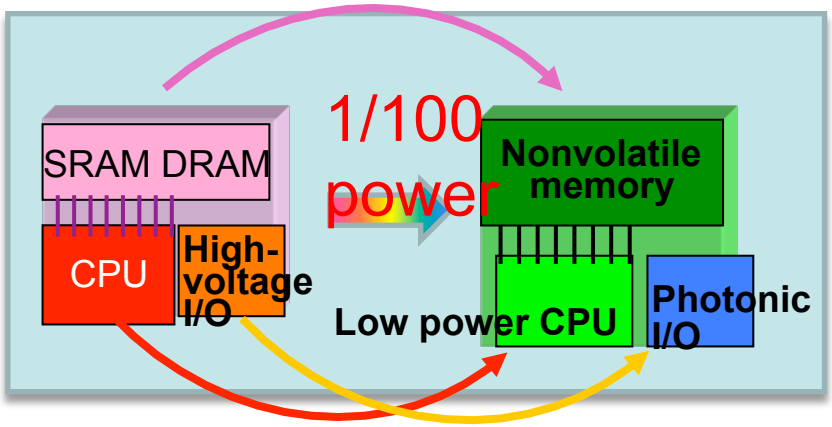
· Low-voltage device LEAP project by Sumihiro

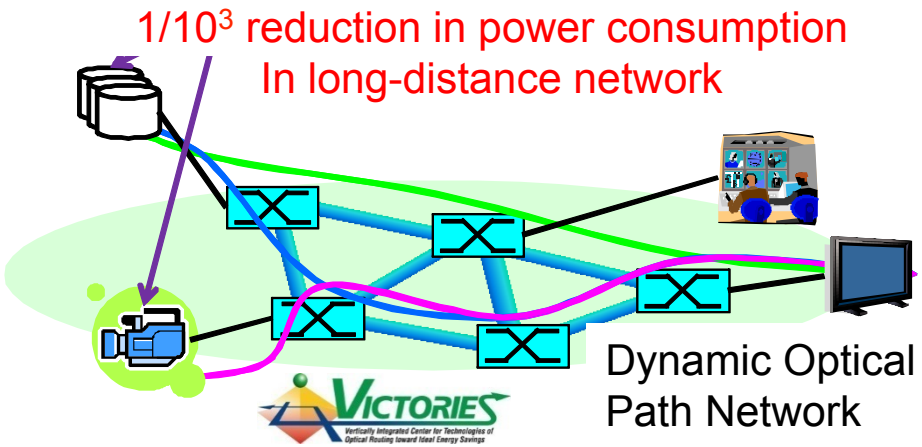
· FIRST, Ultra-low Power Spintronics-based VLSIs by Prof. Ohno, CSIS, Tohoku Univ.

·FIRST project PECST by Prof. Arakawa, Univ. Tokyo

+ PETRA

·VICTORIES project by Dr. Ishikawa



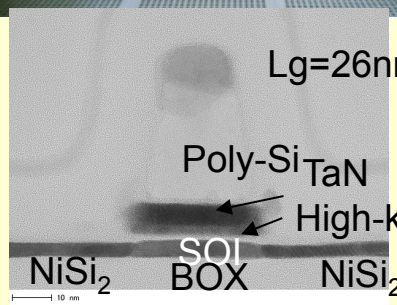


SuperClean Room (SCR) and NanoProcessing Facility (NPF) as a platform for nanoelectronics

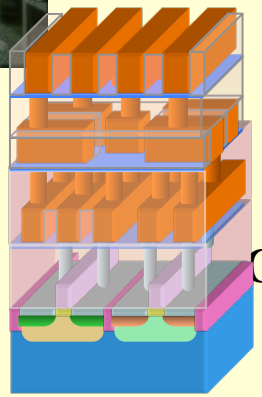
TIA nano

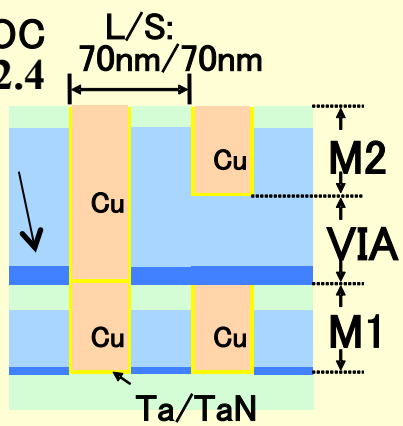
NPF
(NanoProcessing Facility)

SCR: 300 mm wafer process



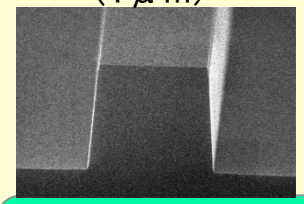
Transistor
- High-k/metal gate
- FD SOI
- Metal Source/Drain





Cu Dual-Damascene

Si optical waveguide
(1 μm)



CMOS platform

Simulation
(TCAD)

Measurement
Characterization

Silicon photonics

other facilities in AIST | NIMS | Univ. Tsukuba | KEK