Nanoelectronics in Japan and TIA
Part 3 of 5

October 17 2013

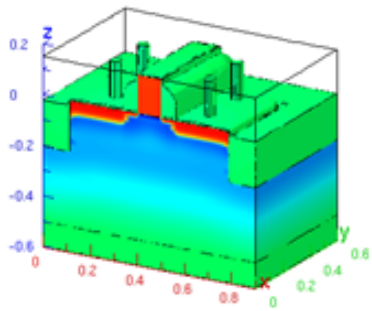
Shigeo Okaya AIST

3D TCAD HyENEXSS

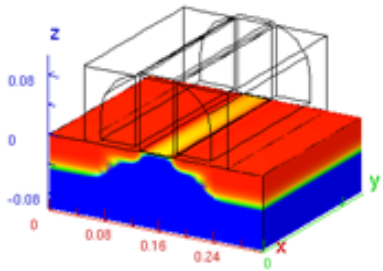
3D TCAD system HyENEXSS

Process Simulator
HySyProS

Device Simulator
HyDeLEOS



MOSFET structure & dopant profile



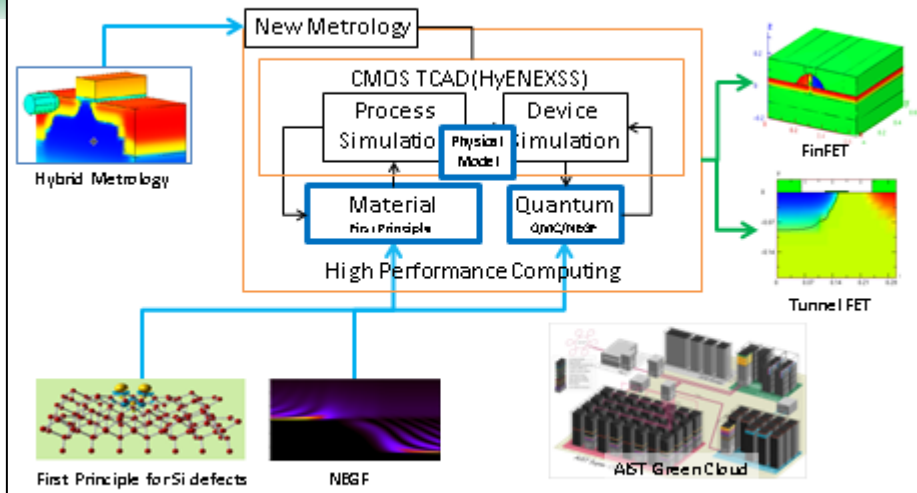
MOSFET electron concentration

Developed in Selete 1996~2011

Collaboration of Japanese Major Semiconductor Companies

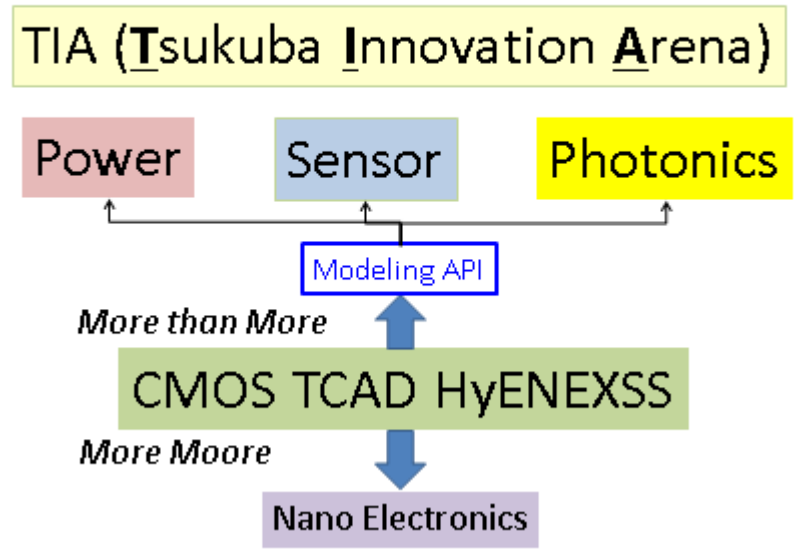
HyENEXSS is mainly CMOS oriented

Next Generation TCAD for Nano-Devices



Collaboration of STARC & AIST

TCAD for More than Moore



Toward nano-generation.

- ✓ Peta-scale Computing.
- ✓ Material & Quantum models
- ✓ TCAD-Hybrid Metrologies.

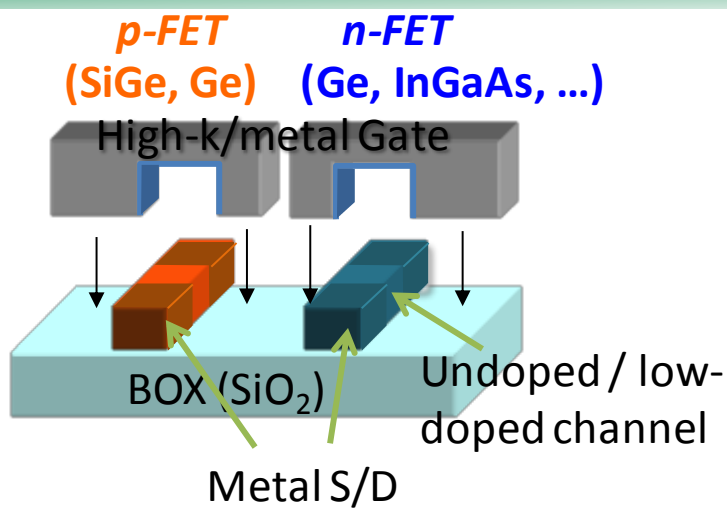
For more than Moore devices.

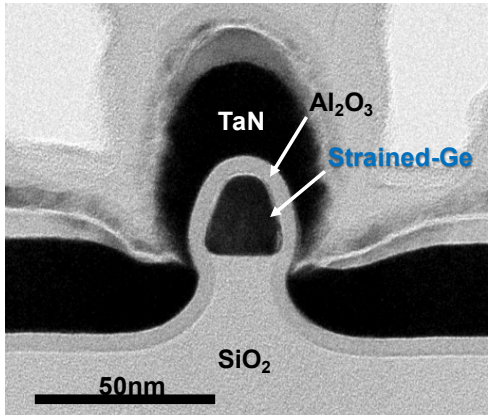
- ✓ New materials.
- ✓ New physics.

Infrastructure of TIA-project.

High-mobility Channel CMOS for Low-voltage Operation

Nanowire CMOS

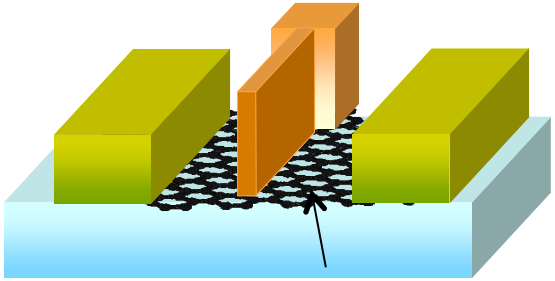




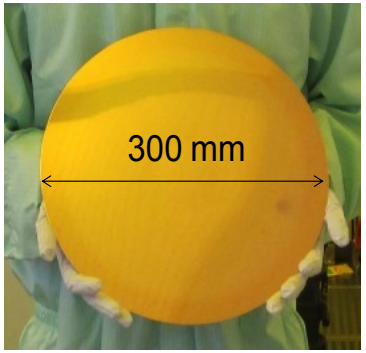
60 nm gate pFET with strained-Ge nanowire: 20 nm thick

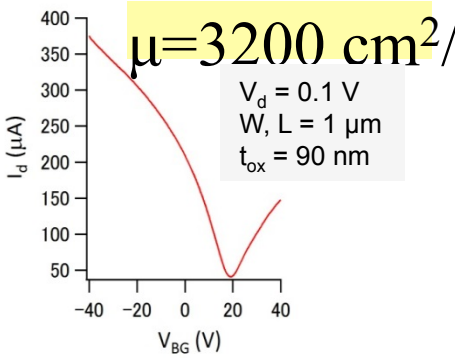
- 4X higher hole mobility than that for a conventional strained Si-pMOSFET

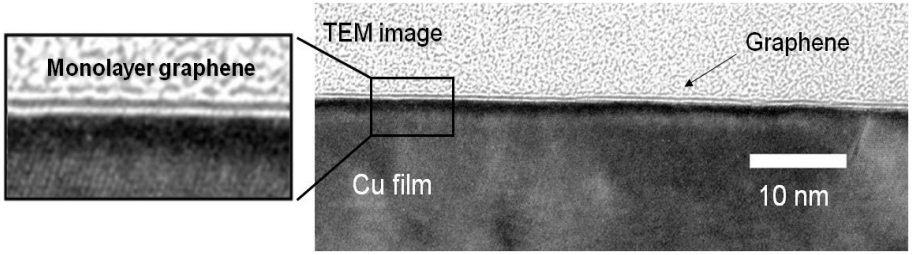
Nanocarbon CMOS



graphene







- Uniform CVD growth of monolayer graphene over 300mm Si wafer.

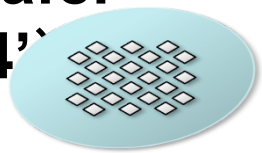
BEOL Post-Si CMOS technology

Post-Si active layer transfer

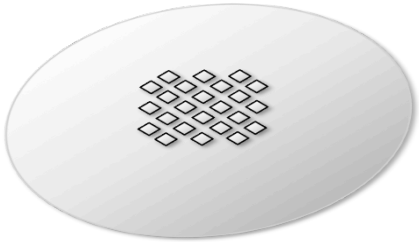
BEOL post-Si device fabrication

III-V/Ge chip
~ 100nm

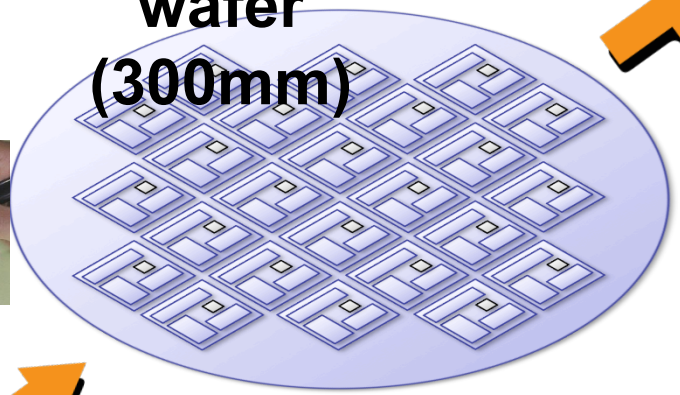
III-V wafer
(2', 4')

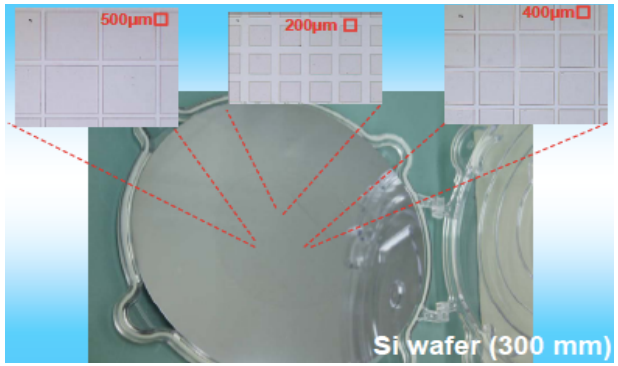


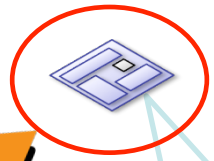
Ge
wafer
(4', 6')



III-V/Ge & Si Hybrid
wafer
(300mm)







III-V/Ge & Si
Hybrid Chip

III-V/Ge device
on Si CMOS