VSIA's
SIP Reuse Standards
Extending International Standards to China
Facilitate Safe SIP Trading

Larry Rosenberg, Consultant
VSIA VP Engineering

How is VSIA involved with Safe Trading in China? Talk Roadmap

- VSIA is the official standard for SIP Reuse in China
  - How did this happen?
  - Why was VSIA chosen?
  - Who is VSIA?
    - What motivated the creation of VSIA in 1996?
    - What are the key concepts behind VSIA Specifications?
    - What Specification and Standards has VSIA released?
  - How does VSIA fit into the current SIP Ecostructure?
  - What are key current focused activities of VSIA?
    - QIP: Quality of IP Metric
    - Tagging SIP blocks
      - Protection and logistics benefits
    - BoM (Bill of Materials): Next Generation Deliverables
  - China CSIG Agreement
    - Deliverables Checklist
    - QIP Certification of SIP
  - Productivity Gap Revisited

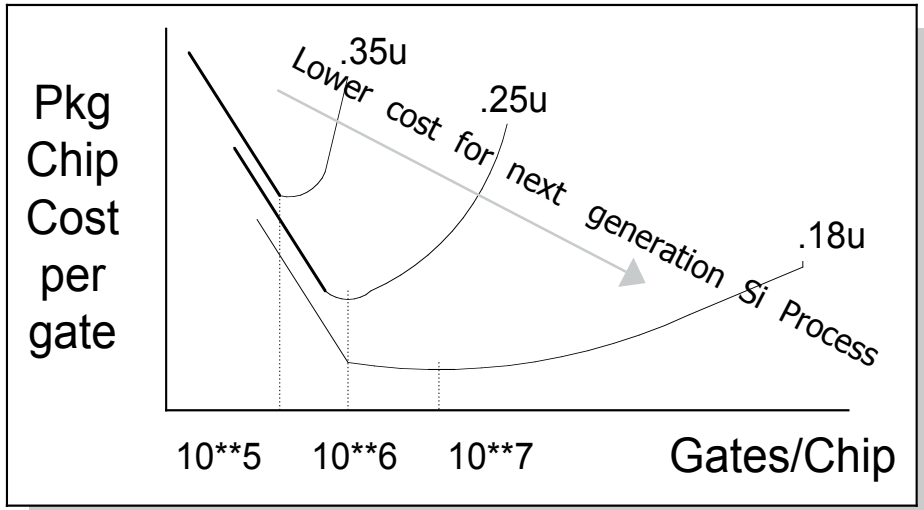
Extension of "Worldwide standards" to China

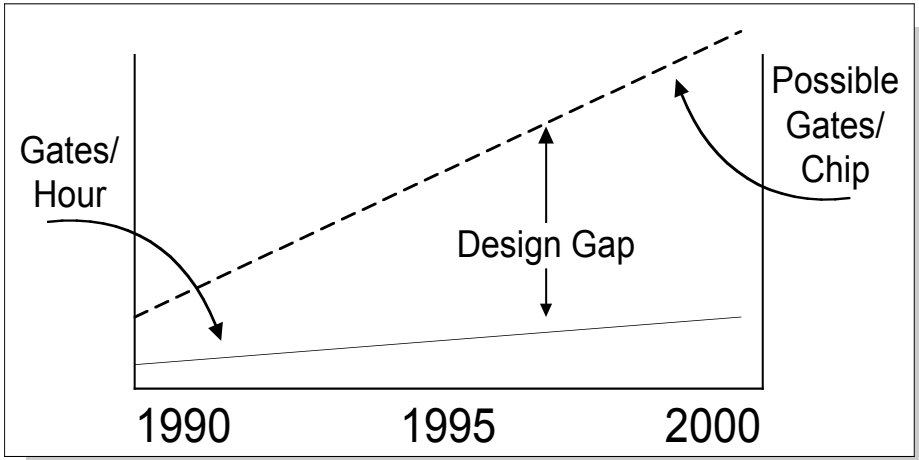
- China has decided to base their SIP Reuse Standards on VSIA
  - NOT "roll their own" (~WAPI) nor simply copy!
    - i.e. China is committed to doing this legally
    - Key visionaries want to play by International Rules
    - They are Paying VSIA a Licensing Fee for right to translate VSIA documents to Chinese and distribute in China
  - Signed the CSIG Agreement
    - Whole collection of cooperation and mutual benefit
    - Two year negotiation finally signed based on **TRUST**
  - Creating collaboration projects: DC, QIP and BoM
- China wants to proactively contribute to
  - SIP Reuse Standards Worldwide (opposite of WAPI!)
  - "Secure Infrastructure" to support enforcement standards (GCSIPTC based in HK)
    - Technical
    - Legal
- **They Want/Need VSIA QIP Certification within China**
  - **Quality is one SIP Access Enabler**

Motivation for VSIA

(1996 Slide: The Growing Design Productivity Gap)

- Million Gate Silicon now
  - 10 million gates by 2000
- Each Silicon Generation provides lower cost (at a higher complexity)
  - So we have to move to next generation
- But the design gap is growing
  - 10 X productivity gain
  - 1000 X silicon gain
- Solution is Design Reuse
  - Requires Spec of Deliverables
  - Requires standard interfaces
  - Requires new design methods
  - Requires Verifiable VCs
- VSIA founded to help
  - And we did!

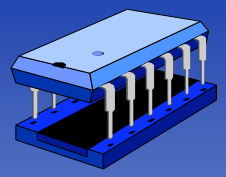




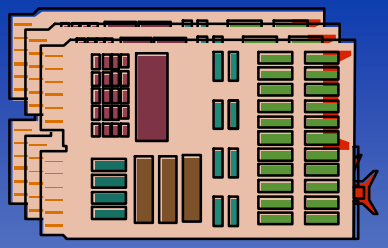
Enabling efficient markets for efficient IP Reuse

Virtual Components enable SoC

Today



Physical Components

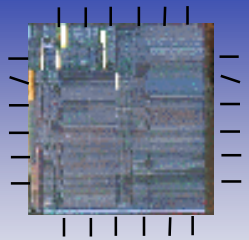


ASIC /ASSP Design

System-Board Integration

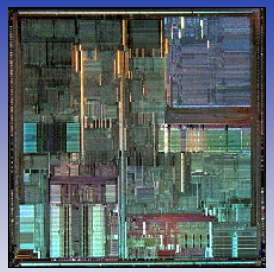
Mix and Match of VCs (design reuse) is an essential part of the solution!

VSIA Vision



Virtual Components

Predictable, Pre-verified 'Virtual Components'

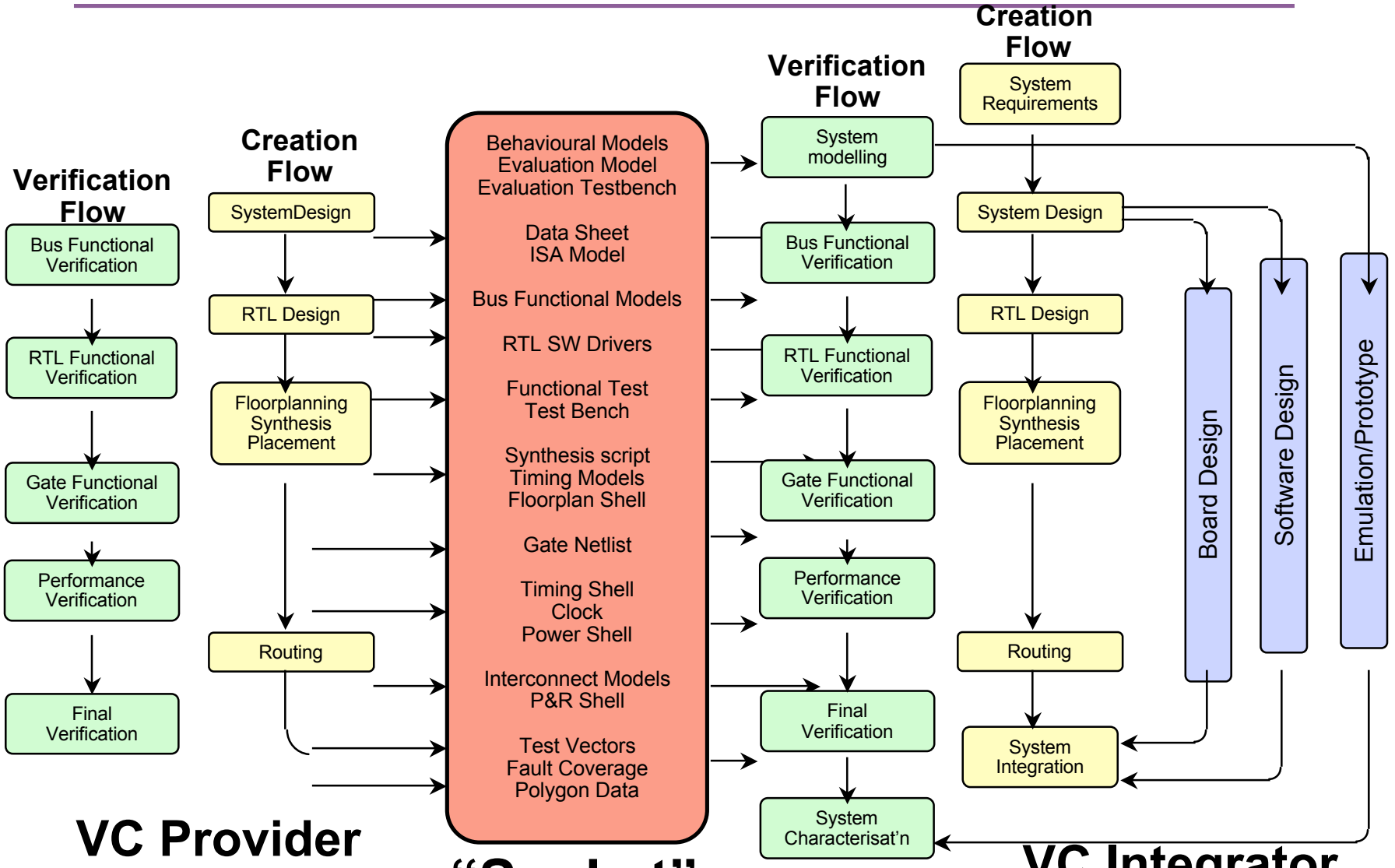


VC/Block Authoring

System-Chip Integration

Virtual Components imply "Reuse without Rework"

Virtual Socket Interface



Enabling efficient markets for efficient IP Reuse

VSI Alliance™

Available VSIA Documents

- Analog/Mixed-Signal Extension Version 2 (AMS 1 2.x)
- Analog/Mixed-Signal Signal Integrity Extension Version 1(AMS 2 1.x)
- On-Chip Bus Attributes Version 1 (OCB 1 2.x)
- Soft & Hard VC Modeling Version 2 (I/V 1 2.x)
- Test Data Interchange Version 1 (TST 1 1.x)
- Virtual Component Transfer Version 2 (VCT 1 2.x)
- VSIA Architecture Document
- System-Level Design Model Taxonomy (SLD 2 2.x)
- Taxonomy of Functional Verification (VER 1 1.x)
- IP Protection White Papers (IPP 1 1.x), (IPP 2 1.x), (IPP 2 1.x)
- System-Level Interface Documentation Standard Version 1 (SLD 1 1.x)
- Test Access Architecture Standard Version 1(TST 2 1.x)
- Virtual Component Attributes (VCA) Version 2 (VCT 2 2.x)
- VC Identification Physical Tagging Standard (VCID) Version 1 (IPP 1 1.x)
- Virtual Component Interface Standard (VCI) Version 2 (OCB 2 2.x)

Specifications
Documents
Standards

Naming Convention: [DWG]_[doc#]_[version].[Revision]

A Sample of VSIA Members (in 2003)

- Advantest
- Agere Systems
- Alcatel
- Analog Devices
- ARC International
- ARM
- Barcelona Design
- Beijing Hongei Electronic Technology
- Beijing Microelectronics Technology Institute
- Cadence Design Systems
- Canadian Microelectronics
- Cannon
- Denso Corp
- Design and Reuse
- ECSI
- Elixent Ltd.
- ETRI Microelectronics Tech Lab
- Hewlett-Packard
- IBM Microelectronics
- IMEC
- Infineon Technologies
- Intel
- Jet Propulsion Laboratory
- Korea Electronics Tech Institute
- LogicVision
- LSI Logic
- Matsushita
- Mentor Graphics
- Motorola SPS
- NEC Electronics
- Oki Electric
- Philips Semiconductors
- Renesas
- Samsung Electronics
- Sanyo
- Seiko Epson
- SIPAC
- STARC
- ST Microelectronics
- Synopsys
- Taiwan SoC Consortium
- LM Ericsson
- THOMSON multimedia
- Toshiba
- TSMC
- UMC

and our Board:

- Agere
- Alcatel
- Cadence
- IBM
- Infineon
- Mentor Graphics
- Motorola
- Sonics
- ST Microelectronics
- TSMC

[new/ /old]

- *The "new" board Members have been added since April, 2003*
  - *They have joined the "New VSIA"*
  - *(because of the new direction)*

Enabling efficient markets for efficient IP Reuse

VSI Alliance™

Summary: Who has been VSIA?

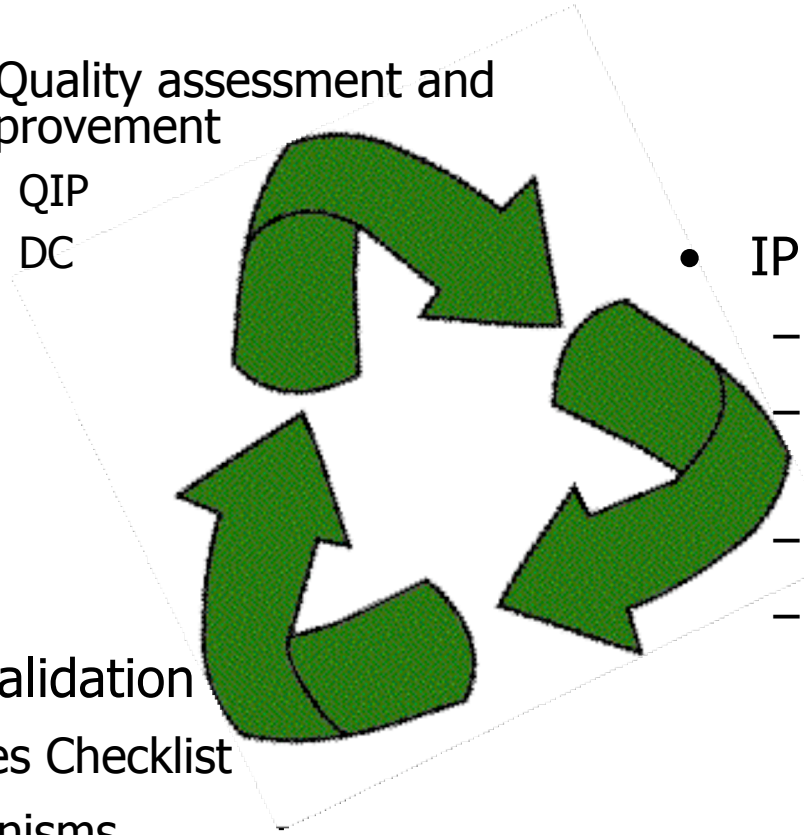
- VSIA's Role in SIP Reuse Standards
  - VSIA "Invented" (popularized/standardized) SIP Reuse in 1996
    - vs. Behavioral Synthesis
  - VSIA has created 6 specs, 5 Standards and 4 "documents" with 12 DWGs
    - But many were good "academic" works
      - But didn't address 'points of pain" nor get to Adoption
- VSIA now has increased focus & relevance with 3 Pillars directed to real-world problems
- Extension of "Worldwide SIP Standards" to China
  - China is becoming a key player in the HW world
    - Decision to adopt worldwide SIP Reuse Standards (VSIA)
      - And it also desperately needs Developed-World SIP

VSIA's new Focused Activities

- VSIA has focused down to three areas
  - QIP Quality SIP Metric
    - has generated high interest and is a foundation for other tools
  - IP Value Protection
    - (Short term) is focused on deploying **Tagging**
  - IP Transfer and Validation
    - Packaging and a common schema structure also provide value by reducing cost of discovery and integration
- These address real world problems and provide immediate solutions
- Communications with peer groups to help create coherence & synergy
  - Si2 –IP Tagging WG created to study integration into OpenAccess
  - Spirit – Tagging, Packaging and BoM interest
  - FSA – HIP QIP
  - CSIG/HKUST
    - adopters and contributors
    - especially to Deliverables Checklist

The Tripod of VSIA Value

- IP Quality assessment and Improvement
  - QIP
  - DC



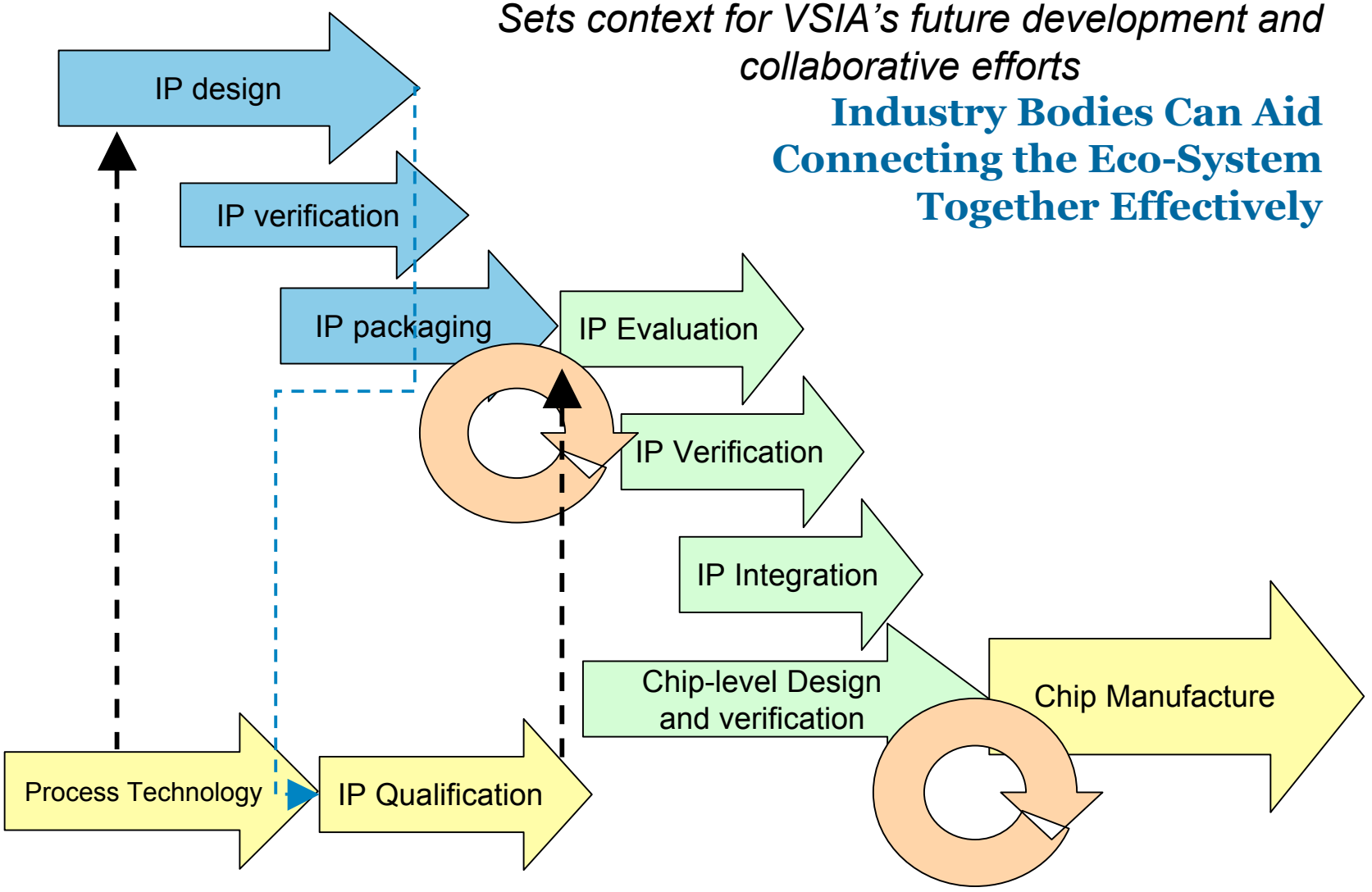
- IP Value Protection
  - Hard and Soft Tagging
  - Incremental Delivery (trust development)
  - Encryption
  - Watermarking

- IP Transfer and Validation
  - BoM/Deliverables Checklist
  - Transfer mechanisms
  - Incremental Delivery

New SIP ECO System with Multiple Handoff Points

Sets context for VSIA's future development and collaborative efforts

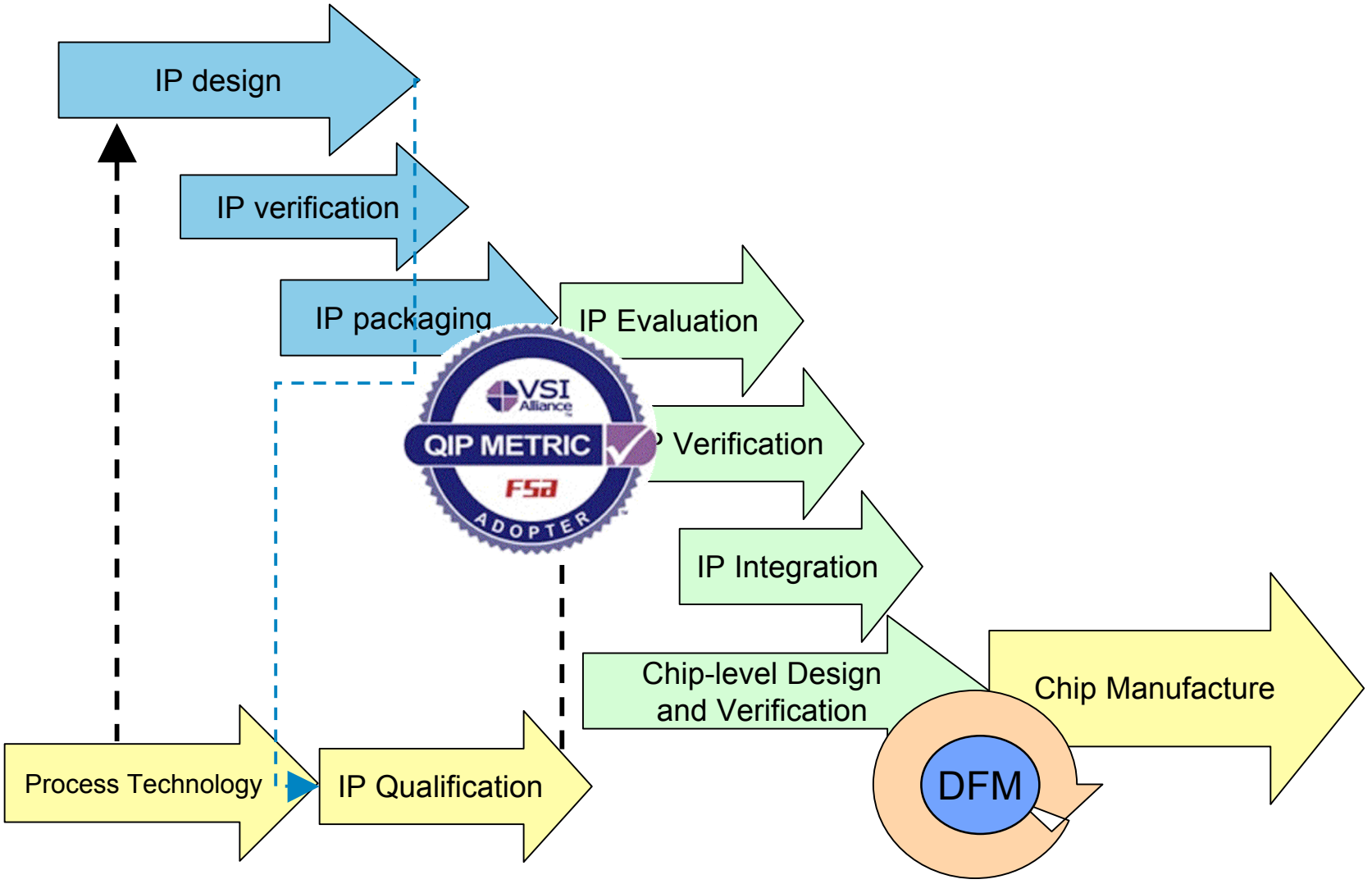
Industry Bodies Can Aid Connecting the Eco-System Together Effectively



Enabling efficient markets for efficient IP Reuse

[1]Raminderpal Singh, *Building an efficient ecosystem*, EE Times (10/10/2005)

VSI Alliance QIP – in the IP ECO System



What is QIP and Why it's Important

- QIP is an interactive SIP Quality Spreadsheet
  - It captures key SIP Design Creation and Integration Requirements
  - It's self scoring
- It's a third generation Metric
  - And consolidates the best features of prior attempts
  - "If you can't beat them, join them"
- It is an objective, verifiable measure of SIP Quality
- It can be used as a Technical Due Diligence Checklist

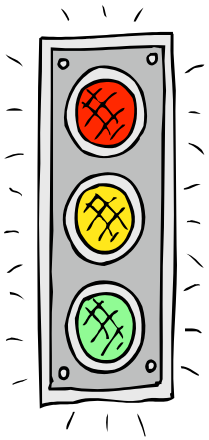
Spreadsheet Goals

- Usable by an IP provider for:
  - a simple checklist of quality factors & metrics
  - individual VC quality evaluation
  - input to IP Integrators for evaluation
- Usable by the IP Integrator / customer for:
  - evaluation of a single VC or whole SoC
  - comparison of VCs from several IP providers
  - weighting the attributes for specific application/company

QIP Organization

- Hierarchical qualification
  - **Vendor Assessment:** Applicable at global level
    - Processes
    - Methodology
    - Infrastructure
    - General capabilities
  - **IP Integration Assessment**: Items most relevant for the successful INTEGRATION of the IP
    - Documentation
    - Deliverables
    - Maturity
  - **IP Development Assessment**: Items most relevant for the successful DEVELOPMENT of the IP
    - Internal documentation
    - Design detail
    - Verification

Standard QIP Metric Concepts



- Relative Importance
  - Fixed for IP providers to provide quantitative baseline measure of IP
    - Imperative: must be met
    - Rule: should be met
    - Guideline: good practice
  - Customizable by IP integrators to reflect their business drivers
- Scoring
  - At-a-glance indicator
  - Individual summary for each sheet

QIP – Ongoing work in VSIA and Collaboration

- The open release (V.2) includes Soft Digital IP & Vendor Qualification
  - Now freely available to Members and Non-Members of VSIA
- Many generations of QIP to finally get it "right"
  - Based on VSIA work + OpenMORE + ChartReuse
- Additional areas of QIP Metric coverage:
  - Hard IP in concert with FSA
  - Verification IP – Working Group launched
  - Software IP
  - Libraries
- Encouragement of adoption beyond traditional community
  - Hong Kong – SIP Platform/Ecosystem for safer SIP "transactions"
  - CSIG (China SIG for VSIA)
    - licensed right to translate legacy VSIA Standards as foundation for China's "recommended" standards; and is adopting the QIP
    - Proposed **QIP Certification**
  - Tutorials, papers, conferences, and press in traditional community

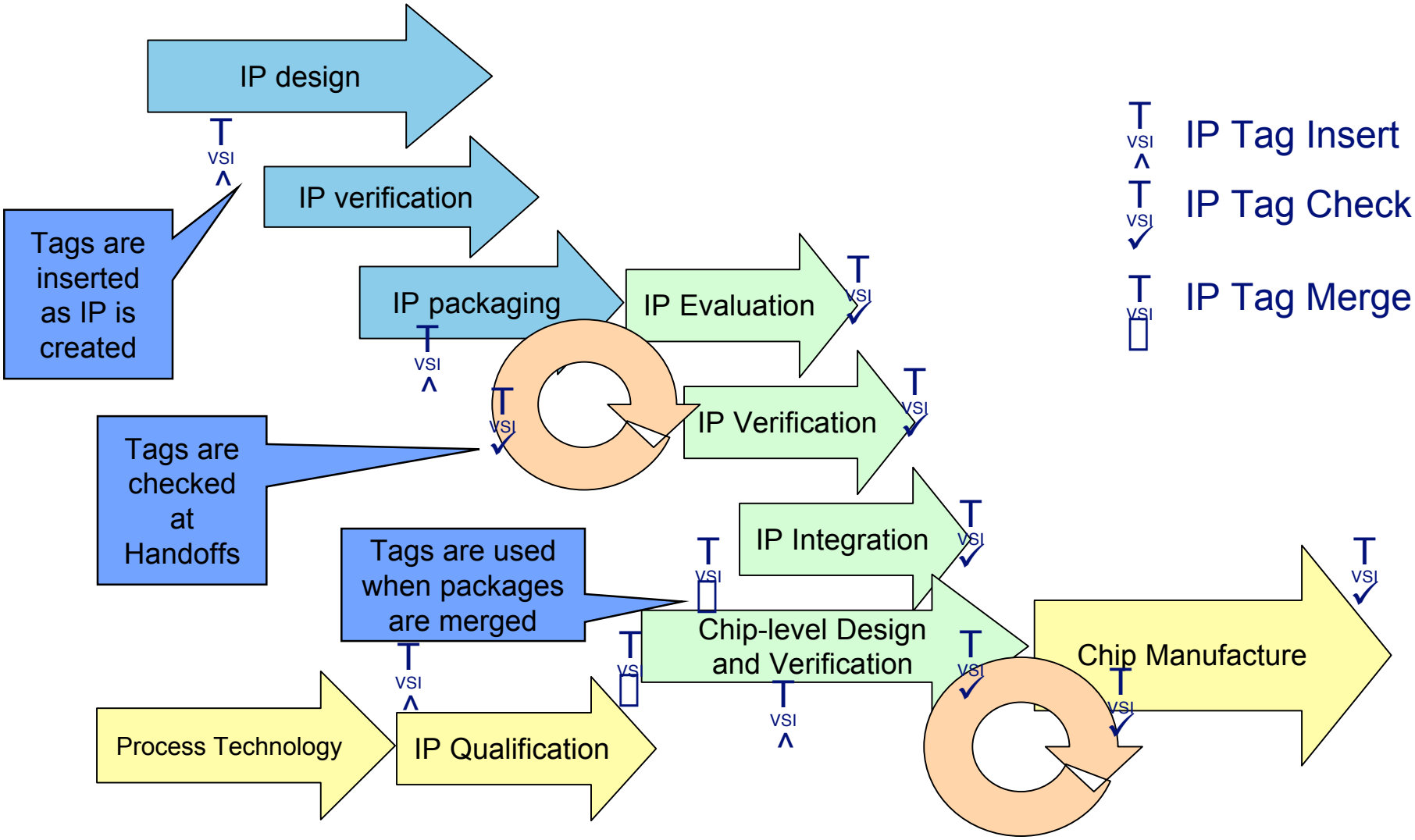
VSI IP Tagging Aids logistics and protection

- VSI has produced 2 standards for data "tags" in IP:
  - Hard IP tagging: for saving tag information in GDS2
  - Soft IP tagging: for inserting converting-&-maintaining tags in soft IP on it's journey to fab
- The tags contain
  - Producer/Responsible party
  - Version information
  - Tool chain and tool version used
- The tags are used for:
  - Assurance – is the version of IP that is used clear of bugs, are all the deliverables from the same version
  - Providence/Tracking – Providence is being able to track the history of an IP
  - Identification – who will fix the bugs? Who is paid, and why?
  - Protection - Helps keep honest people honest
    - No inadvertent fabrication of illegal chips
- The tags provide benefit to:
  - The IP producer: Able to identify the use of and versions used
  - The System integrator: Able to match deliverables with assurance
  - The Foundry: Able to track back to the source for issues and payments
- The standards benefit all of these groups and the EDA tool vendors as well
  - EDA tool requirements are reduced when the standard is adopted by all

Enabling efficient markets for efficient IP Reuse

Working with Spirit and SI2 to proliferate Tagging

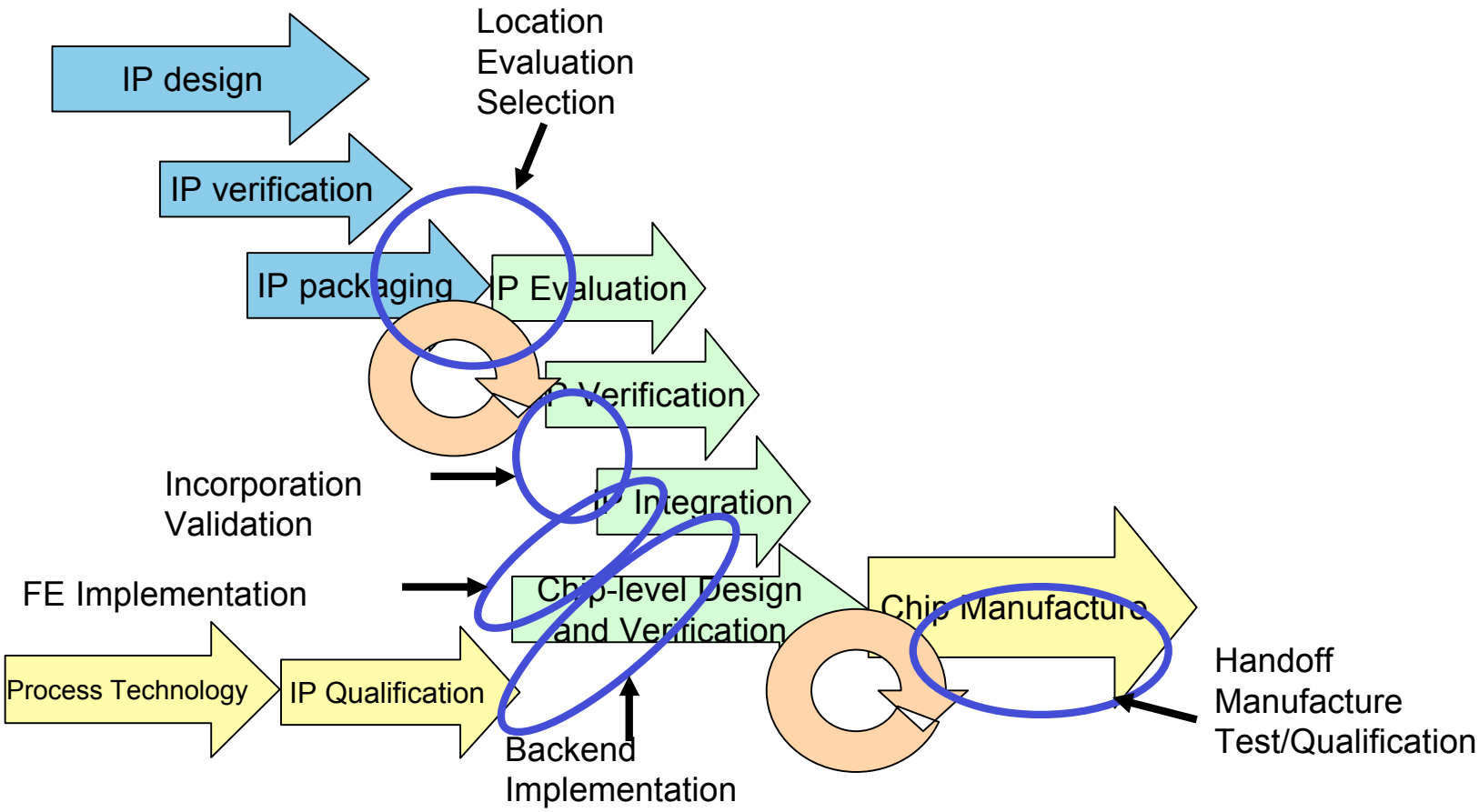
The IP ECO System – Tagging flow



Deployment/Transfer sequence for BoM

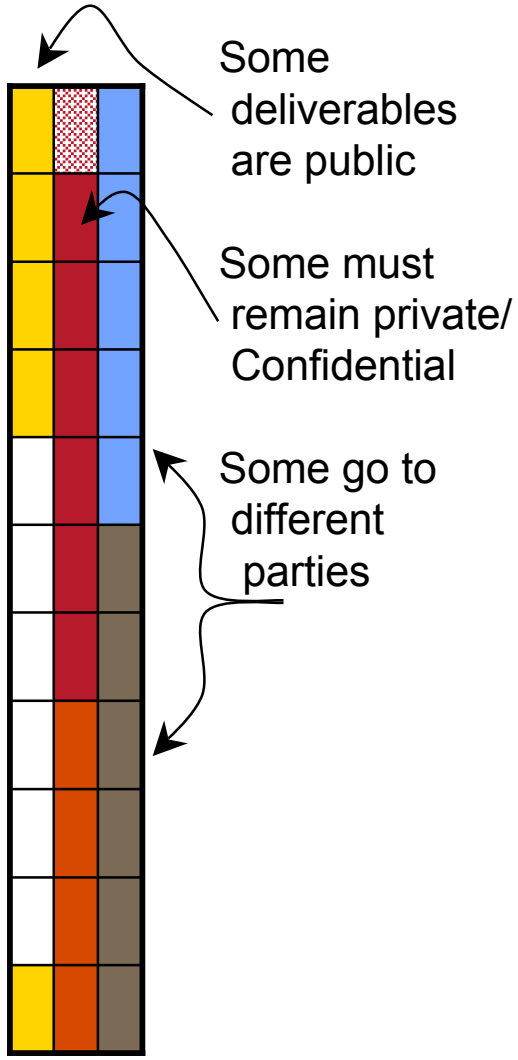
The Development, Deployment and use of IP follows this sequence.

Each step has different requirements and own Deliverables



Deployment chain for BoM

Each step	different Deliverables needs
• Location /Discovery	Catalog entry
• Evaluation	QIP & Eval BoM
• Selection	QIP & Eval BoM
• Incorporation	Frame and component views – Inc BoM
• Validation	Verification BoM
• FE Implementation	
– Handoff here	Implementation BoM
• Backend Implementation	Physical BoM
• Handoff	Handoff BoM
• Manufacture	
– Handoff here	Implement BoM
• Test/Characterization	Test BoM
• Use	Use Characterization ?



Deliverables Checklist activity ties Quality with Transport

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Need for consistent schema and tools for delivery

- The IP Transport Pillar provides standards facilitating the exchange of IP between providers and consumers.
- Key goals
  - IP design flow automation,
  - incremental IP delivery and
  - IP directory structure remapping.
- The next 2 slides (deleted) had highlighted
  - Schema for deliverables structure
    - Supports transport and BoM
    - Compatible with schema from Spirit to facilitate collaboration
  - Mechanisms for transferring SIP between designs with different hierarchies

VSIA Activities in China

The CSIG (China Special Interest Group for VSIA)

- Signed "CSIG Agreement" in Beijing August 23, 2005 with CSIA and CSIP
- Agreement has two features
  - Licenses VSIA "foundation" documents for China's "Recommended" IP-Reuse Standards
  - Creates CSIG
    - China Special Interest Group for VSIA
      - To facilitate the creation of **Chinese IP-Reuse Standards based on VSIA** and then promote these standards and VSIA within China
      - Conduit of VSIA Docs to IPCG Standards Group
      - **Provide a forum for discussion of IP Reuse issues in China**
      - Consists of *normal* VSIA Members, 35 "Selected Companies" and 20 IP-Reuse Researchers
      - Defining areas and mechanism of collaboration
        - Challenges but strong trust over-coming issues
      - **QIP Certification (Proposal)**

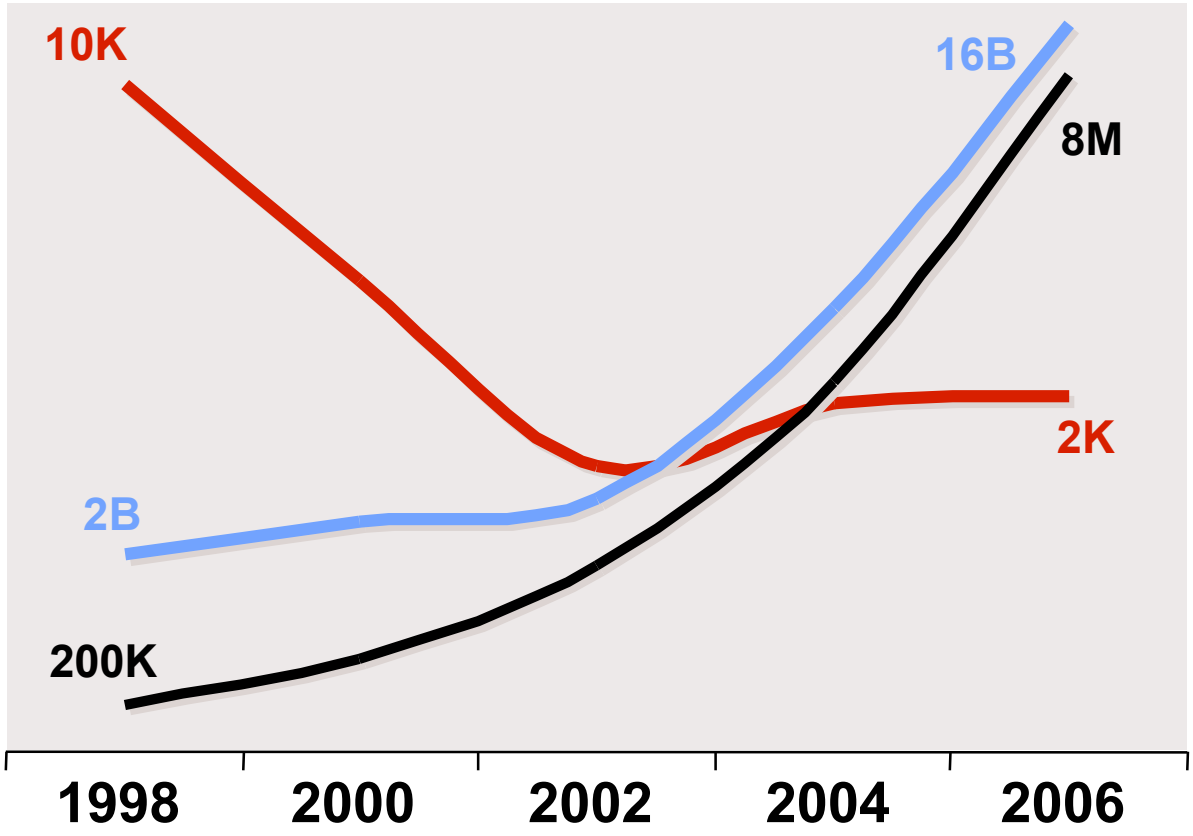
CSIG - Vision and Charter

- VSIA Vision:
  - dramatically accelerate system chip development by specifying open standards
- CSIG Vision:
  - dramatically accelerate system chip development in China by specifying Chinese open standards fully compatible with international standards
- VSIA Message
  - *Enabling efficient markets for efficient IP Reuse*
- CSIG Charter and Message
  - Help develop the SoC/IP Reuse Infrastructure/EcoSystem in China
    - *Enabling efficient SoC markets in China for efficient IP Reuse*
- "Kam" Xie Xuejun is "Secretary General" of the CSIG
  - He is an Assistant Manager at CSIP and former Ph.D. student of Professor Ye
- Plans
  - Website Capability
    - Host Chinese Version of VSIA Standards
  - Coordinate China's Collaboration with VSIA for BoM/DC/QIP Development,Collaboration and Deployment within China

VSIA QIP Certification

- Deep concern about SIP Quality, authenticity and infringement
  - GCSIPTC Project addresses these
- First Step will be technical
- Will encourage use of QIP
  - But Concern about "grade inflation"
  - Therefore want VSIA QIP Certification
  - Sponsored by CSIA (with full MII support)
- HKUST developed Deliverables Checklist
  - Links Deliverables with QIP Line Items
    - Use QIP Line items under license from VSIA
  - License DC back to VSIA
  - Have own proprietary Software to support DC
    - Automatic verification of subset of QIP and DC line items
      - Will help kick start the Audit process for certification
  - **Interest expressed In US and Europe to help support**

Design Complexity becoming Disruptive



Starts

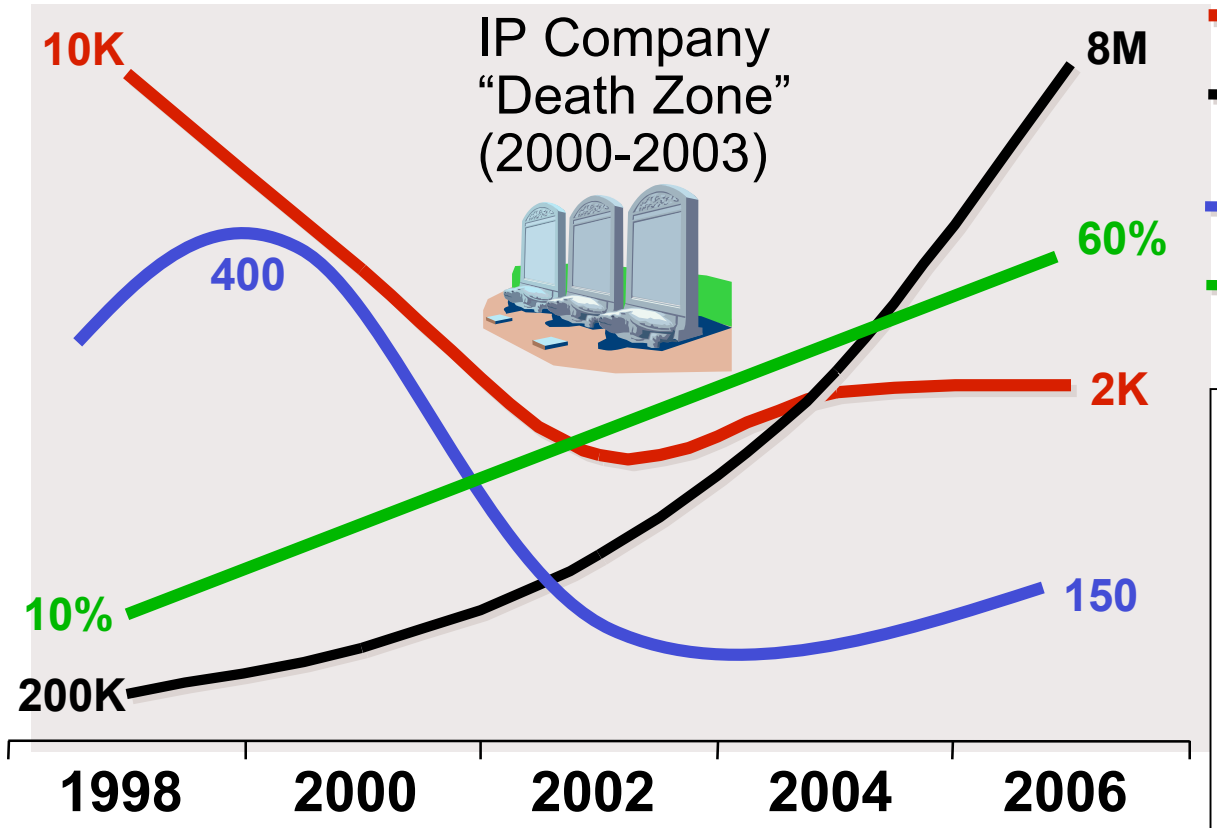
Gates/IC

Total Gates

T = S x G

Source: iSuppli

IP Companies & Design Reuse



Source: Warren Savage, IPextreme Inc.

Starts

Gates/IC

 # IP Companies

% Gates from IP

- **Design reuse**
  - Steadily increases
  - But slower than expected due to available engineers
  - Semi's start building reuse infrastructure and training
- **IP companies can't survive**
  - Fewer design starts
  - Fierce price competition

Enabling efficient markets for efficient IP Reuse

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Summary of key points

- VSIA Activity now focused in three areas that have impact
  - QIP Quality
  - IP Value Protection
  - IP Transfer and Validation
- China is basing their SIP Reuse standards on VSIA
  - CSIG Agreement
    - Legally licenses VSIA Standards
    - Creates CSIG activity
  - VSIA QIP Certification
  - All this effort is motivated and driven by the "GCSIPTC" Project
  - Ongoing Collaboration with China based on growing trust
    - Most important for any success
  - Design Gap may reappear as Challenge
    - **And drive increased SIP Reuse and "trade"**